5 Field Effect Transistors

INTRODUCTION

Field effect transistors (FET) are devices which work on the principle of "field effect". Field effect refers to the process of modulation of longitudinal current flow between two terminals of the device by a transverse electric field applied to the third terminal.

There are different techniques by which field effect is realized. Based on this FETs may be of different types - junction field effect transistor (JFET), metal-semiconductor field effect transistor (MESFET), metal-insulator field effect transistor (MISFET) etc. MISFET is commonly known as MOSFET, because the insulator usually used is an oxide (SiO_2). It is also called insulated gate field effect transistor (IGFET), because the gate is insulated from the channel through which current flows.

Field effect transistors are unipolar devices. The current flow is by one type of charge carriers (majority carriers) only. As minority carriers are not involved in the conduction process generation/recombination noise is not present in field effect devices. These devices have high input impedance as the input is usually applied across a reverse-biased p-n junction or across a metal oxide semiconductor interface. FETs are less temperature dependent and more immune to radiation. Fabrication of field effect devices are simpler (less number of steps) than bipolar devices. They occupy less area on the chip.

As FETs are immune to radiation, they are used in amplifiers required for satellite communication in the GHz frequency range. Because of high input impedance, they are suitable for input stages of operational amplifiers, instrumentation amplifiers etc.

In JFET, the field effect is obtained by the voltage applied across a p-n junction. In MESFET, the field effect is obtained by the voltage applied across'a metal semiconductor rectifying contact. In MOSFET, the voltage is applied across a metal-insulator (oxide) semiconductor interface to obtain the field effect.

5. 1 JUNCTION FIELD EFFECT TRANSISTOR

A simplified structure of a JFET is shown in Fig. 5.1. It consists of a lightly doped n-region sandwiched between two p^+ (heavily doped p) regions as shown in Fig. 5.1. The middle 'n' region is the channel of the JFET and the p^+ regions form the gates. A JFET with n-type channel is called n-channel JFET.

One end of the channel is designated as source and the other end as drain. Usually the source and drain are interchangeable. For n-channel JFET, the terminal to which higher potential is applied acts as the drain. The drain collects the charge carriers emitted from the source through the channel. The gate terminal controls the flow of current through the channel.

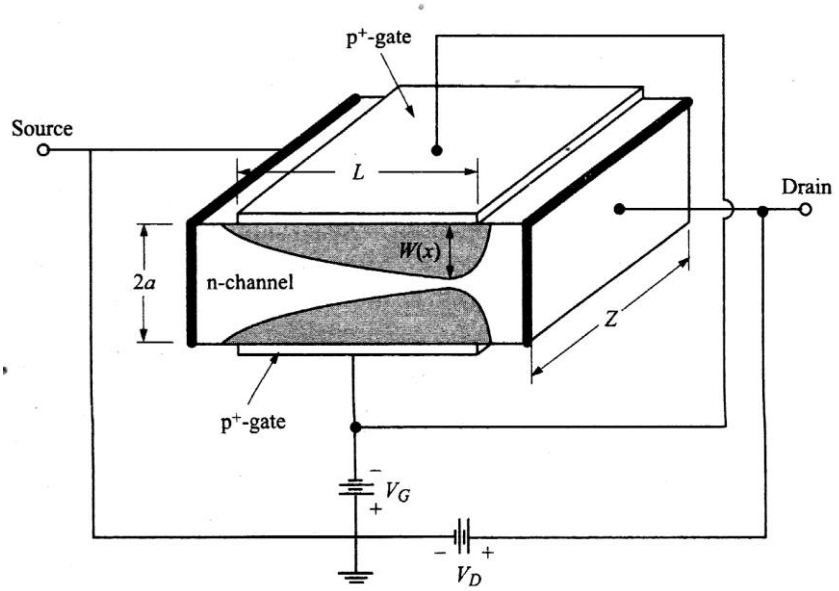


Fig. 5.1 Simplified structure of a JFET

The actual structure of a dual JFET is shown in Fig. 5.2(a). The dual JFET fabrication process starts with a p^+ substrate. A thin layer of n-region is epitaxially grown over the substrate, p^+ gate region is diffused over this after growing oxide and etching window. The n^+ source and drain regions are formed by diffusion. Ohmic contacts are formed for various regions.

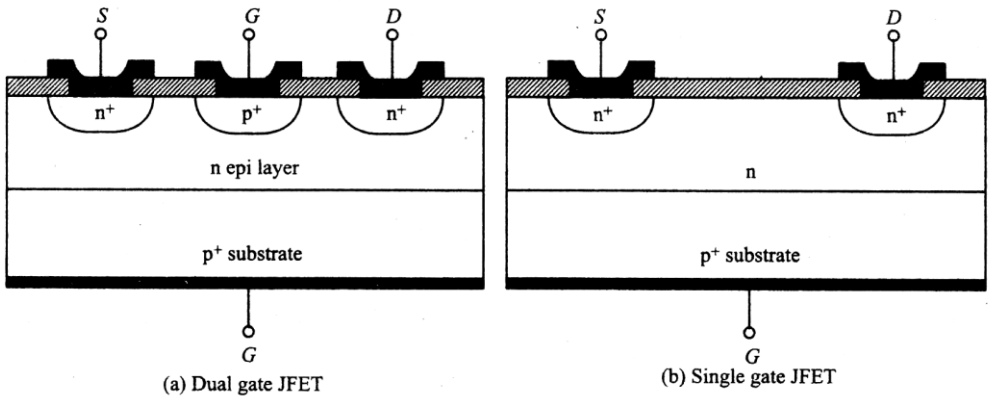


Fig. 5.2 Actual structure of a JFET

The single gate structure is similar to the dual gate structure except for the p^+ gate diffusion as in Fig. 5.2(b).

Principle of operation

A simplified schematic structure of a dual gate n-channel JFET is shown in Fig. 5.3. The gate regions are heavily doped and the channel is lightly doped. The dimensions of the device are as given below.
Channel thickness - 2a
Channel width -Z
Channel length -L

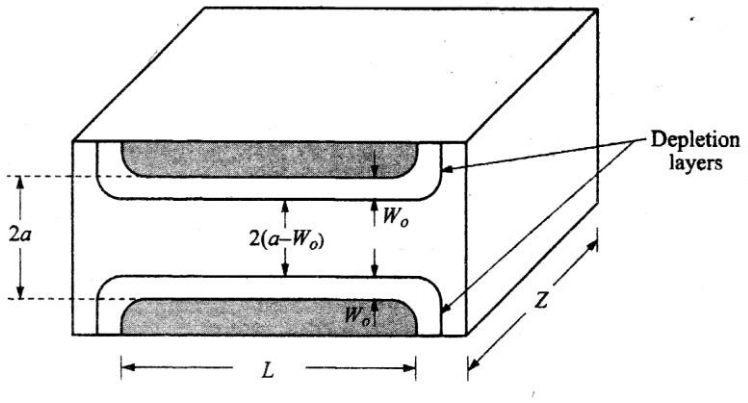


Fig. 5.3 Simplified structure of a dual JFET showing the equilibrium depletion layer width and channel thickness

Let the channel doping be N_D and Wo be the depletion layer width of gate to channel junction on one side under thermal equilibrium.
The resistance of the channel with no bias (V_{GS} = 0, V_{DS} = 0) or under thermal equilibrium is given by

$$R_0 = \frac{\rho L}{A} = \frac{L}{\sigma A} \text{ ,where}$$

$$\sigma = qN_D\mu_n$$

$$A = Z(2a - 2W_0) = 2Z(a - W_0)$$

$$\text{Q } R_0 = \frac{L}{2qN_D\mu_n Z(a - W_0)} \tag{5.1}$$

$$G_0 = \frac{1}{R_0} = \frac{2qN_D\mu_n Z(a - W_0)}{L} \tag{5.2}$$

where G_0 represents conductance of the channel at equilibrium and

$$W_0 = \sqrt{\frac{2\grave{o}V_0}{qN_D}}$$

where V_0 is the built in potential of gate to channel junction.

The resistance of the channel can be varied by varying the gate voltage. Gate acts as the control terminal. With increase in reverse-bias on the gate, depletion layer extends more into the

channel. Therefore, the effective channel thickness and the channel cross-section reduces, decreasing channel conductance. The change in conductance by the change in gate voltage is known as conductance modulation.

When a drain to source voltage is applied, the drift current through the channel (I_D) is governed by Ohm's law ($I_D = \frac{V_{DS}}{R}$). The resistance R is controlled by gate voltage (V_{GS}). It also changes with drain to source voltage as explained below.

Assume an ideal JFET structure with gate regions extending from end to end of the channel as shown in Fig. 5.3.

Drain Characteristics

Drain characteristics is the plot of drain current (I_D) as a function of drain to source voltage (V_{DS}) keeping gate to source voltage (V_{GS}) constant, as shown in Figs. 5.9 and 5.11.

(a) $V_{GS} = 0$; $V_{DS} = 0$ (Fig. 5.4)

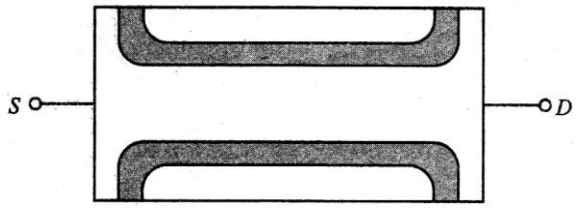
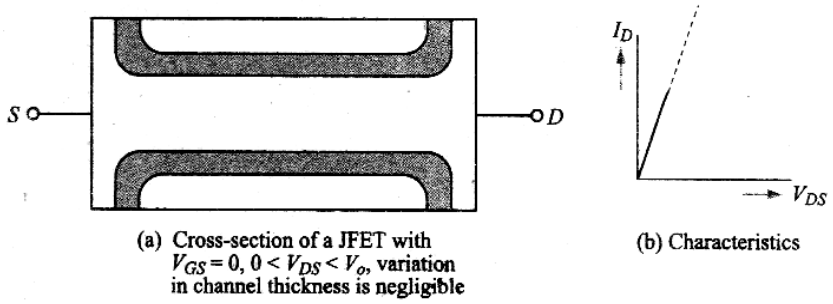


Fig. 5.4 Cross-section of a JFET with $V_{GS} = 0$ $V_{DS} = 0$

$R=R_0$; $I_D = 0$

(b) $V_{GS} = 0$; $0 < V_{DS} < V_o$ (very small V_{DS}) (Fig. 5.5)



(a) Cross-section of a JFET with $V_{GS} = 0$, $0 < V_{DS} < V_o$, variation in channel thickness is negligible

(b) Characteristics

Fig. 5.5

For small values of V_{DS}, the change in channel resistance is negligible i.e., resistance remain almost constant (R_0). Therefore, dram current increases linearly with increase in V_{DS}. This portion of the characteristics is called linear region or ohmic region.

(c) $V_{GS} = 0$; $V_0 < V_{DS} < V_{D(sat)}$ (Fig.5.6)

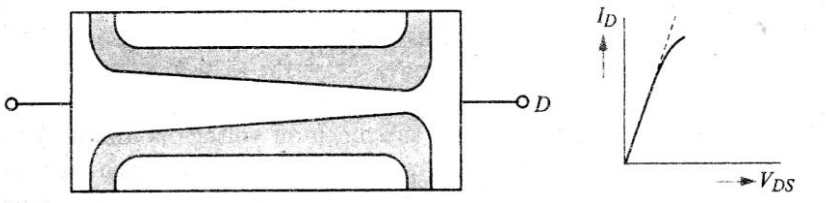


Fig. 5.6 Cross-section of a JFET at V_{GS} == 0; V_o < V_{DS} < V_D(sat)

As V_{DS} increases further, voltage drop in the channel gradually increase from source end to drain end. Therefore; the reverse-bias between gate and channel gradually increases from source end to drain end. As a result the depletion layer width gradually increases from source end to drain end. This increases the effective resistance of the channel.

As the channel resistance increases with increase in V_{DS}, the slope of the characteristics decreases. (Slope of characteristics is the reciprocal of channel resistance $\frac{\Delta I_D}{\Delta V_{DS}} = \frac{1}{R}$).

(d) V_{GS} = 0; V_{DS} = $V_{D(sat)}$ (Fig. 5.7)

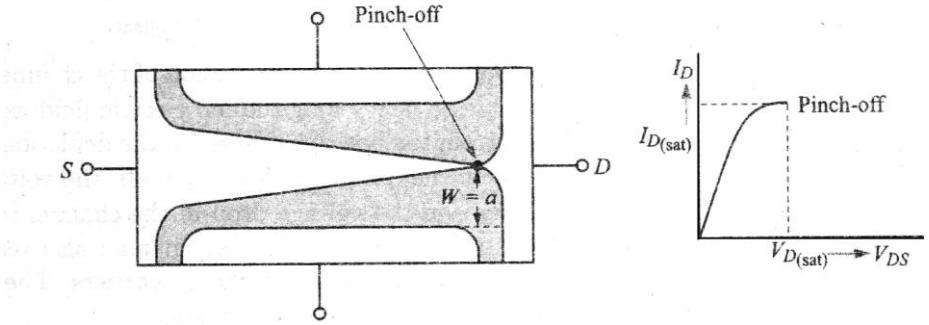


Fig. 5.7 Cross-sectional view of JFET at V_{GS} = 0; V_{DS} = $V_{D(sat)}$

As V_{DS} is increased gradually the depletion layers at the drain end of the channel just meet together, reducing the effective channel thickness to zero. This condition is called pinch-off. Under this condition the drain end of the channel is just pinched-off.

The pinch of voltage (V_p) of a JFET is the voltage between the drain end of the channel and the gate at the onset of pinch off. It is also equal to the minimum reverse bias between drain end of channel and gate at which the channel thickness become zero at the drain end.

The voltage between the drain-gate p-n junction at pinch off may be expressed as

$$V_p = V_0 + V_{D(sat)} - V_{GS}$$

The drain to source voltage at which pinch-off occurs changes with change in V_{GS}. But V_P is independent of V_{DS} or V_{GS}. It is unique for a given JFET. The drain to source voltage at which drain end of the channel just pinches off is called saturation voltage ($V_{D(sat)}$). Thus $V_{D(sat)}$ varies with change in V_{GS}.

The width of the depletion layer at pinch-off equals half width of the channel.

i.e., at pinch off W(x = L) = a

Therefore at pinch-off $W = a = \sqrt{\frac{2\grave{o}V_P}{qN_D}}$

or $$V_P = \frac{qN_D a^2}{2\grave{o}} \qquad (5.3)$$

This expression for V_P indicates that the pinch-off voltage is unique for a given JFET and it depends on the channel doping and channel width. Pinch-off voltage increases with increase in channel doping and channel width. If the channel doping is more, the penetration of depletion layer into the channel will be less for a given reverse-bias.

(e) $V_{GS} = 0$; $V_{DS} > V_{D(sat)}$ (Fig. 5.8)

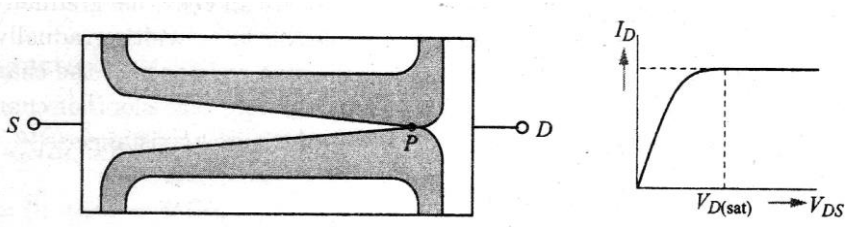


Fig. 5.8 Cross-section of JFET with $V_{GS} = 0$; $V_{DS} > V_{D(sat)}$

If drain to source voltage is increased beyond pinch-off, more portion of the channel gets pinched-off. After pinch-off the current is due to heavy longitudinal electric field existing in the channel. This electric field originates from the positive charges in the depletion layer (ionised donor) and terminates on electrons in the channel. After pinch-off, the voltage in excess of $V_{D(sat)}$ drops in the depletion layer and the voltage drop in the channel remains almost constant. Therefore, the supply of charge carriers into the channel also remains almost constant. The drift current depends on the number of charge carriers. Therefore after pinch-off the current through the channel remains almost constant.

(f) Avalanche break down

At high values of V_{DS}, the reverse-biased gate channel junction breaks down due to avalanche multiplication as shown in Fig. 5.9.

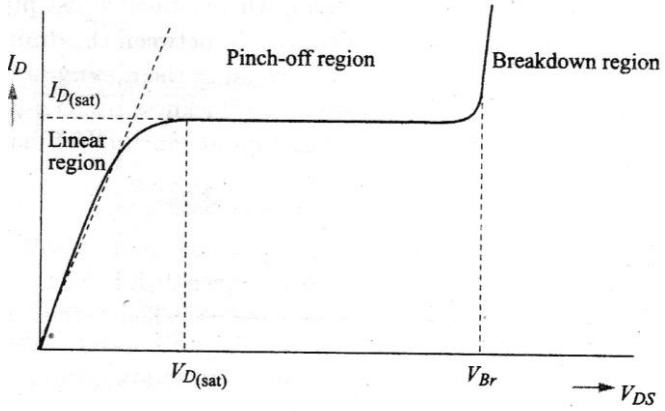


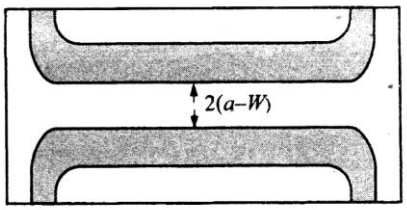
Fig. 5.9 Characteristics of a JFET for $V_{GS} = 0$ showing different regions of operation

(g) Effect of change in V_{GS} (Fig. 5.10)

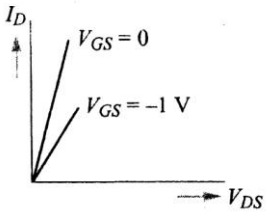
An increase in V_{GS} (reverse-bias) increases the depletion layer width and channel resistance. This reduces the slope of the characteristics in the initial ohmic or linear region. It also reduces the value of $V_{D(sat)}$ (drain to source voltage at which pinch-off takes place).

Now, the V_{DS} required to pinch-off the drain end is less by V_{GS}.

i.e., $V_{D(sat)} = V_P - V_0 + V_{GS}$ (Notice that V_{GS} is negative)



(a) Cross-section of a JFET with $V_{GS}<0$, and $V_{DS} = 0$



(b) Effect of change in V_{GS} on drain characteristics in the linear region

Fig. 5.10

With increase in V_{GS}, V_{DS} at which avalanche breakdown occurs also decreases. The value of V_{GS} at which channel gets completely depleted is called cut-off voltage or threshold voltage of JFET.

The complete drain characteristics of JFET is shown in Fig. 5.11.

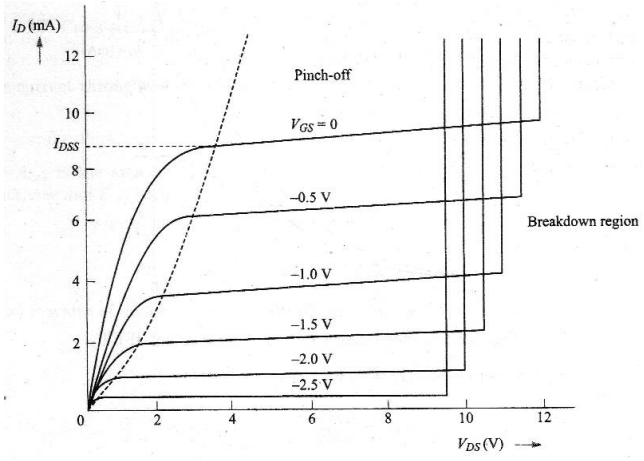


Fig. 5.11 The drain characteristics of an n-channel JFET

The dynamic drain resistance,

$$r_D = \left.\frac{\Delta V_{DS}}{\Delta I_D}\right|_{V_{GS\ (constant)}}$$

A JFET is operated as a small signal amplifier, oscillator etc., in the pinch-off region. JFET can be used as a voltage variable resistor in the linear region as the resistance vary linearly with gate source voltage.

Transfer characteristics

Transfer characteristics is the plot of drain current as a function of gate to source voltage (I_D vs V_{GS}) keeping V_{DS} constant. Keeping V_{DS} constant, if reverse bias between gate and source is increased the drain current decreases as shown in Fig. 5.12. The drain current is maximum when $V_{GS} = 0$ (minimum channel resistance). The drain current reduces to zero when $V_{GS} = V_{GS(cut\text{-}off)}$

$$V_{GS\,(cut\text{-}off)} = V_o - V_P$$

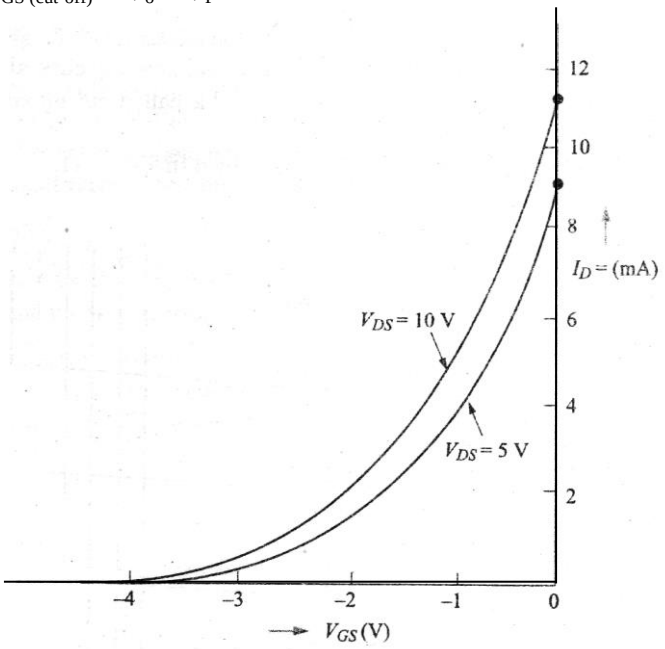


Fig. 5.12 Transfer characteristics of n-channel JFET

The slope of the transfer characteristics gives transconductance g_m of the device as

$$g_m = \left.\frac{\Delta I_D}{\Delta V_{GS}}\right|_{V_{DS\ (constant)}}$$

It can be observed that g_m increases with increase in I_D.

5.1.2 Static I-V Characteristics (Derivation)

The deviation of static I-V characteristics is based on the following approximations:

(1) The mobility in the channel remains constant (independent of electric field).

(2) The gate and channel are uniformly doped and doping in the gate region is much higher than that in the channel.

(3) The length of the channel (L) is large compared to its thickness 2a. Therefore, the transverse electric field is large compared to electric field along the direction of current in the channel. On applying V_{DS}, the voltage drop in the channel gradually increases from the source end to drain end. This approximation is called *gradual channel approximation.*

(4) Applied drain to source voltage is less than or equal to $V_{D(sat)}$

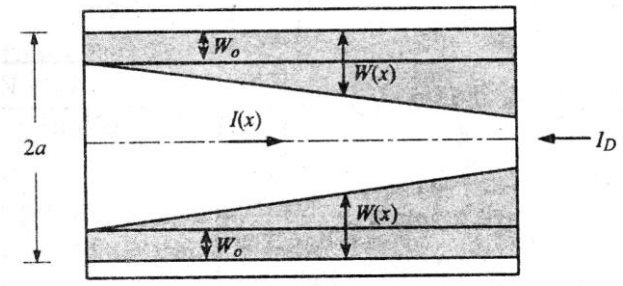


Fig. 5.13 Cross-section of a JFET showing the direction of currents and variation of depletion layer width along the channel

The current through the channel is given by

$$I_{(x)} = A_{(x)}\sigma E_{(x)} \tag{5.4}$$

where $A_{(x)}$ is the area of cross-section of the channel at distance x, σ is the channel conductivity and $E_{(x)}$ is the electric field at x in the channel.

$$A_{(x)} = 2(a\text{-}W(x))Z$$
$$= 2Z(a\text{-}W(x))$$

W(x) is width of depletion layer at distance x from source end.

$$W(x) = \sqrt{\frac{2\grave{o}\left[V_{(x)} + V_0 - V_{GS}\right]}{qN_D}} \tag{5.5}$$

where $[V_{(x)} + V_0 - V_{GS}]$ represents the reverse-bias between channel and gate at distance x.

$\sigma = qN_D\mu_n$ (Channel is n-type with $N_D >> n_i$)

Drain current $I_D = -I_{(x)}$

$$= - A_{(x)}\sigma E_{(x)}$$
$$= -2Z\,[\,a - W(x)]\,qN_D\mu_n \frac{-dV_{(x)}}{dx}$$
$$= 2\,qN_D\mu_n Z\left[a - \sqrt{\frac{2\grave{o}\left(V_{(x)} + V_0 - V_{GS}\right)}{qN_D}}\right]\frac{dV_{(x)}}{dx}$$

Integrating the above expression from source to drain,

$$\int_0^L I_D dx = \int_0^{V_{DS}} 2qN_D\mu_n Z\left[a - \sqrt{\frac{2\grave{o}\left(V_{(x)} + V_0 - V_{GS}\right)}{qN_D}}\right] dV_{(x)}$$

$$I_D[x]_0^L = \int_0^{V_{DS}} 2qN_D\mu_n Za\left[1 - \sqrt{\frac{2\grave{o}\left(V_{(x)} + V_0 - V_{GS}\right)}{qN_D a^2}}\right] dV_{(x)}$$

$$I_D L = \int_0^{V_{DS}} 2qN_D\mu_n Za\left[1 - \sqrt{\frac{\left(V_{(x)} + V_0 - V_{GS}\right)}{V_P}}\right] dV_{(x)}$$

($\therefore \quad V_P = \frac{qN_D a^2}{2\grave{o}}$ by equation (5.3))

$$I_D = \frac{2qN_D\mu_n Za}{L}\left[V_{(x)} - \left(\frac{\left(V_{(x)} + V_0 - V_{GS}\right)}{V_P}\right)^{3/2} \times \frac{2}{3}V_P\right]_0^{V_{DS}}$$

$$= \frac{2qN_D\mu_n Za}{L}\left[V_{DS} - \frac{2}{3}V_P\left\{\left(\frac{\left(V_0 - V_{DS} - V_{GS}\right)}{V_P}\right)^{3/2} - \left(\frac{\left(V_0 - V_{GS}\right)}{V_P}\right)^{3/2}\right\}\right]$$

$$= G_o\left[V_{DS} - \frac{2}{3}V_P\left\{\left(\frac{\left(V_0 - V_{DS} - V_{GS}\right)}{V_P}\right)^{3/2} - \left(\frac{\left(V_0 - V_{GS}\right)}{V_P}\right)^{3/2}\right\}\right] \qquad (5.6)$$

Where G_0 is the equilibrium channel conductance

$G_0 = \frac{2q\mu_n N_D Za}{L}$ (Neglecting W_0 in equation (5.2))

Threshold Voltage

Threshold voltage (V_{th}) is the voltage that must be applied to the gate to completely deplete the channel or to reduce the channel thickness to zero. At this condition channel resistance is infinitely high and the current is zero for any V_{DS}.

$$V_{th} = V_0 - V_p$$

Drain Current at Saturation

The drain current at saturation ($I_{D(sat)}$) is obtained by replacing V_{DS} with $V_{D(sat)}$ in Eqn. (5.6) Therefore equation (5.6) becomes

$$I_{D(sat)} = G_0\left[V_{D(sat)} - \frac{2}{3}V_P\left\{\left(\frac{\left(V_0 - V_{D(sat)} - V_{GS}\right)}{V_P}\right)^{3/2} - \left(\frac{\left(V_0 - V_{GS}\right)}{V_P}\right)^{3/2}\right\}\right] \qquad (5.7\ a)$$

$$= G_0 \left[V_P - V_o + V_{GS} - \frac{2V_P}{3} + \frac{2V_P}{3} \left(\frac{(V_0 - V_{GS})}{V_P} \right)^{3/2} \right]$$

($Q\ V_p = V_{D(sat)} + V_0 - V_{GS}$) (5.7b)

Note: JFET is not used with a forward-bias to gate, as it results in a very low-input impedance.

Channel conductance (g_D)

$$g_D = \frac{1}{rD} = \left. \frac{\partial I_D}{\partial V_{DS}} \right|_{V_{GS\ (constant)}}$$

Differentiating equation (5.6) with respect to V_{DS},

$$g_D = G_o \left[1 - \left(\frac{(V_o + V_{DS} - V_{GS})}{V_P} \right)^{1/2} \right] \quad (5.8)$$

In the linear region; $V_D << (V_0 - V_{GS})$

$$\therefore\ g_D = G_o \left[1 - \left(\frac{(V_o - V_{DS})}{V_P} \right)^{1/2} \right] \quad (5.9)$$

Transconductance (g_m)

$$g_m = \left. \frac{\partial I_D}{\partial V_{GS}} \right|_{V_{DS\ (constant)}}$$

Differentiating equation (5.6) with respect to V_{GS}

$$g_m = G_o \left[\left(\frac{(V_o + V_{DS} - V_{GS})}{V_P} \right)^{1/2} - \left(\frac{V_o - V_{GS}}{V_P} \right)^{1/2} \right] \quad (5.10)$$

At pinch-off, $V_{DS} = V_{D(sat)}$

$$\therefore\ g_m = G_o \left[\left(\frac{(V_o + V_{D(sat)} - V_{GS})}{V_P} \right)^{1/2} - \left(\frac{V_o - V_{GS}}{V_P} \right)^{1/2} \right]$$

$$= G_o \left[1 - \left(\frac{V_o - V_{GS}}{V_P} \right)^{1/2} \right] \quad (Q\ V_0 + V_{D(sat)} - V_{GS} = V_P) \quad (5.11)$$

Equations (5.9) and (5.11) are identical. This shows that drain conductance (g_D) in the linear region equals the transconductance (g_m) in the saturation region.

A relationship connecting drain current with different values of V_{GS} for a JFET may be written as

$$I_{D(sat)} = I_{DSS} \left[1 + \frac{V_{GS}}{V_P} \right]^2 \quad (5.12)$$

where,

$I_{D(sat)}$ = drain to source saturation current at gate source voltage V_{GS}

I_{DSS} - short-circuit drain saturation current i.e., saturation current with $V_{GS} = 0$

V_P - pinch-off voltage (positive for n-channel JFET and negative for p-channel JFET).

V_{GS} - negative for n-channel and positive for p-channel.

Example 5.1 An n-channel silicon JFET at 300 K has width Z == 1 mm, channel thickness on one-side a = 1μm, channel length L = 25 μm, channel doping $N_D = 10^{16} cm^{-3}$ and the gate doping is 10^{19} cm^{-3}. Determine:

a. the contact potential,

b. pinch-off voltage,

c. current at V_{GS} = -2 V, V_{DS} = 3 V and

d. saturation current at V_{GS} = -2 V using theoretical and approximate expressions. Take μ_n = 1100 cm^2/Vs.

Solution

a. $V_0 = \frac{kT}{q} \ln \frac{N_A N_D}{n_i^2}$

$= 0.026 \ln \frac{10^{19} \times 10^{16}}{\left(1.5 \times 10^{10}\right)^2} = 0.877$ V

b. $Vp = \frac{qN_D a^2}{2ò}$

$= \frac{1.6 \times 10^{-19} \times 10^{16} \times \left(1 \times 10^{-4}\right)^2}{2 \times 8.854 \times 10^{-14} \times 11.8} = 7.66$ V

c. $G_0 = \frac{2qN_D \mu_n Za}{L}$

$G_0 = \frac{2 \times 1.6 \times 10^{-19} \times 10^{16} \times 1100 \times 0.1 \times 1 \times 10^{-4}}{25 \times 10^{-4}}$

$= 0.0141$ S

Gate to channel voltage,

$V_{GC} = V_{DS} + V_0 - V_{GS} = 3 + 0.877 + 2 = 5.877 < V_p$

Therefore JFET is not in pinch-off region.

$$I_D = G_0 \left[V_{DS} - \frac{2}{3} V_P \left\{ \left(\frac{(V_o + V_{DS} - V_{GS})}{V_P} \right)^{3/2} - \left(\frac{V_o - V_{GS}}{V_P} \right)^{3/2} \right\} \right]$$

$$= 0.0141 \left[3 - \frac{2}{3} \times 7.66 \left\{ \left(\frac{5.877}{7.66} \right)^{3/2} - \left(\frac{2.877}{7.66} \right)^{3/2} \right\} \right] = 10.47 \text{ mA}$$

$$I_{D(sat)} = G_0 \left[V_P - V_o + V_{GS} - \frac{2}{3} V_P + \frac{2}{3} V_P \left(\frac{(V_o - V_{GS})}{V_P} \right)^{3/2} \right]$$

$$= 0.0141 \left[7.66 - 0.877 - 2 - \frac{2}{3} \times 7.66 + \frac{2}{3} \times 7.66 \left(\frac{7.877 + 2}{7.66} \right)^{3/2} \right]$$

$= 12.01$ mA

$$I_{D(sat)} = I_{DSS}\left(1+\frac{V_{GS}}{V_P}\right)^2$$

$$I_{DSS} = I_{D(sat)}\big|_{VGS=0}$$

$$= 0.0141\left[7.66\text{-}0.877\text{-}\frac{2}{3}\times 7.66+\frac{2}{3}\times 7.66\left(\frac{0.877}{7.66}\right)^{3/2}\right] = 26.4\text{ mA}$$

$$I_{D(sat)} = 92.8\left(1+\frac{(-2)}{7.66}\right)^2 = 14.41\text{mA}.$$

5.1.3 Real JFETs

In the preliminary discussion and derivation of drain current, several secondary effects like channel length modulation, variation of mobility with electric field etc., were neglected. The characteristics of real JFETs differ from ideal ones due to these secondary effects.

(1) Channel length modulation: In ideal model, the drain current remains constant after pinch-off. But in the actual characteristics, it can be observed that the drain current increases slightly with increase in V_{DS} after pinch-off.

The effective length of the channel decreases after pinch-off, as the pinched-off portion of the depletion layer extends more and more towards the source end. This increases the channel conductance ($G_o \alpha \frac{1}{L}$ by equation (5.2)).

The conductance of the channel is modulated by the variation in effective length with change in V_{DS} in the pinch of region. This is called *channel length modulation*. Therefore, the drain current increases with increase in V_{DS}, after pinch-off. This is analogous to base-width modulation in BJT.

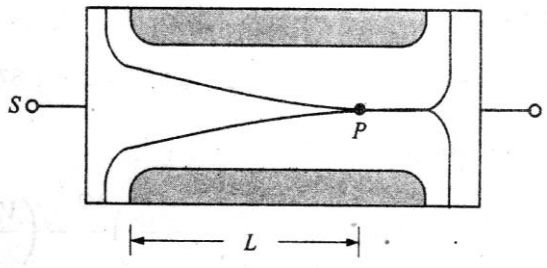


Fig. 5.14 Channel length modulation (as V_{DS} exceeds $V_{D(sat)}$, the effective length of the channel decreases)

(2) High field effects: In short channel devices, the electric field along the channel is very high. Under very high electric field, mobility decreases with increase in electric field (μ= v/E , as velocity saturates at high electric field as explained in Section 1.12). Due to reduction in mobility, conductance of the channel decreases and the current for a given V_{DS} is less than that expected by equation (5.7). High field effects are observed in short channel devices.

(3) Breakdown: In a JFET, the gate channel junction is always reverse-biased. Large values of V_{DS} may cause avalanche breakdown of the junction due to multiplication in the depletion layer. With more negative value of V_{GS}, the breakdown occurs at smaller values of V_{DS} as shown in Fig. 5.12.

(4) Temperature effects: With increase in temperature the mobility of charge carriers decrease due to increased scattering by lattice vibration. This leads to reduction in current with rise in temperature. This effect is in contrast to that in BJT where the collector current increases due to increase in reverse saturation current, which may even lead to thermal run away.

5.1.4 Small signal equivalent circuit

The low-frequency small signal equivalent circuit of a JFET is shown in Fig. 5.15. In the equivalent circuit, the parameters are defined as

$$\text{Transconductance } g_m = \left.\frac{\partial I_D}{\partial V_{GS}}\right|_{V_{DS\ (constant)}}$$

$$\text{Channel conductance } g_D = \left.\frac{\partial I_D}{\partial V_{DS}}\right|_{V_{GS\ (constant)}}$$

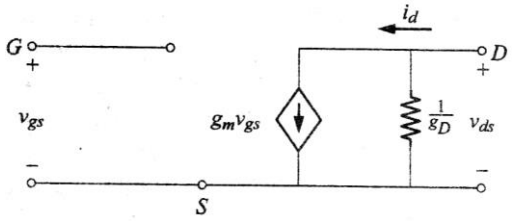


Fig. 5.15 Low-frequency small signal equivalent circuit of a JFET

The open-circuit at the input side represents high input impedence of JFET.

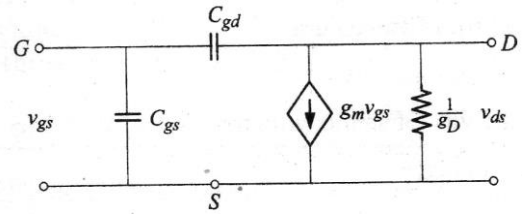


Fig. 5.16 High-frequency small signal equivalent circuit of a JFET

Small signal high-frequency equivalent circuit of a JFET is shown in Fig. 5.16. At high-frequency, the capacitances Cgs and Cgd has to be included in the circuit.

C_{gs} ~ capacitance between gate and source
C_{gd} ~ capacitance between gate and drain.

5.1.5 Figure of Merit (f_r)

The unity gain frequency of a JFET is known as its figure of merit. It is also known as *cut-off frequency.*

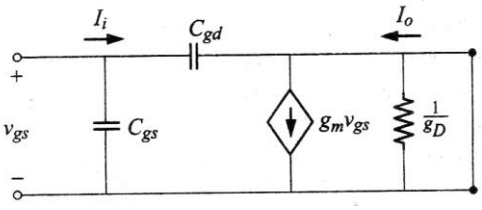


Fig. 5.17 Circuit arrangement to determine figure of merit of JFET

The high frequency equivalent circuit let of a JFET is shown in Fig. 5.17. From the figure,

$$I_i = V_{gs}\, j\omega(C_{gs} + C_{gd})$$

$$I_o = g_m \upsilon_{gs}$$

$$\frac{I_o}{I_i} = \frac{g_m}{j\omega(C_{gs} + C_{gd})} = \frac{g_m}{j2\pi f(C_{gs} + C_{gd})}$$

$$f = f_T \ when \left|\frac{I_o}{I_i}\right| = 1$$

$$\therefore \qquad f_T = \frac{g_m}{2\pi(C_{gs} + C_{gd})} \tag{5.13}$$

The figure of merit of JFET may also be expressed as

$$f_T = \frac{q\mu_n a^2 N_D}{4\pi \grave{o} L^2} \tag{5.14}$$

where,

μ_n	-	electron mobility in the channel
a	-	half width of the channel
N_D	-	channel doping
C	-	permittivity of semiconductor
L	-	channel length

The transit time of JFET is given by

$$\tau_t = \frac{L}{\upsilon_d} = \frac{L}{\mu_n E_{(x)}} = \frac{L^2}{\mu_n V_{DS}} \tag{5.15}$$

where,

υ_d	-	drift velocity of electrons in the channel
V_{DS}	-	Drain to source voltage
$E_{(x)}$	-	electric field in the channel

Equation (5.15) is valid at low electric field where mobility is constant. But at high electric fields drift velocity saturates and mobility decreases.

Therefore, transit time is given by,

$$\tau_t = \frac{L}{\upsilon_s} \tag{5.16}$$

where, υ_s - saturation velocity of electrons.

Factors affecting high-frequency response of a JFET:

(1) Increase in mobility increases f_T: Devices with higher mobility have improved high frequency response. Higher mobility increases drift velocity for a given electric field. So transit time decreases with increase in mobility increasing the speed of the device.

(2) Increase in channel doping increases the high-frequency performances due to increased conductance. But at very high doping, mobility decreases which adversely affect high-frequency response.

(3) Reduction in channel length reduces capacitance, increases transconductance, increasing f_T Reduction in channel length reduce the transit time. The value of channel length is limited

by the technology used for fabrication. Also, if length is very small, velocity saturates due to high electric field and mobility decreases.

5.3 METAL OXIDE SEMICONDUCTOR SYSTEMS

MOS capacitor, MOSFET and charge coupled devices are examples of metal oxide semiconductor (MOS) systems. MOS capacitor is a two terminal MOS device which may be considered as a MOS diode. MOSFET's are field effect transistors which make use of a metal oxide semiconductor interface to modulate conductance of the channel. MOSFET's are superior to BJT's in many aspects such as high scale of integration, high gain band-width product etc., and they find extensive use in high speed digital circuits, high density integrated circuits etc. Charge coupled devices (CCD) consists of basically an array of MOS capacitors and are used as dynamic memories.

5.3.1 MOS Capacitor

A two terminal metal oxide semiconductor system is used as a MOS capacitor (also known as MOS diode). The structure of a metal (Al) oxide (S_iO_2) semiconductor (p-type Si) capacitor is shown in Fig. 5.23.

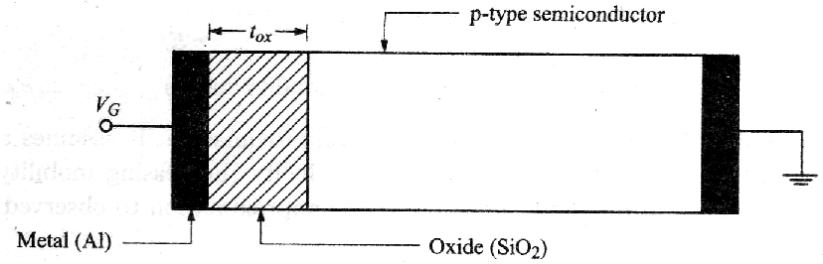


Fig. 5.23 Structure of a MOS capacitor

Ideal MOS Capacitor

A MOS capacitor is considered to be ideal if (1) the work function of metal and semicon- ductor are equal, (2) oxide is a perfect insulator with no trapped charges, no defects and no interface states. The equilibrium energy band diagram of such a system is shown in Fig. 5.24.

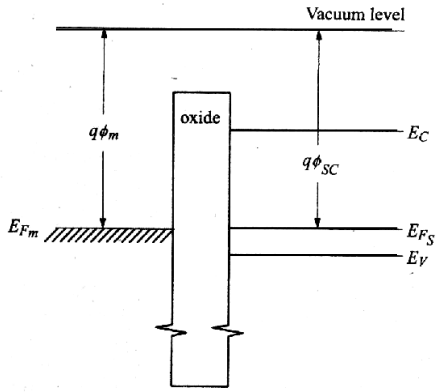


Fig. 5.24 Equilibrium energy band diagram of a MOS capacitor

Tips to draw energy band diagram of MOS systems:

(1) At equilibrium Fermi level is a common horizontal line.
(2) When a bias is applied, Fermi level on the semiconductor side moves up or down relative to that in the semiconductor.
(3) The oxide conduction band and valence band bends in the direction of applied electric field.
(4) With any bias, the relative positions of E_C, E_V and E_i remain unchanged with respect to oxide conduction band edge at the interface.
(5) The relative position of Fermi level in the neutral region of semiconductor remains unchanged with respect to E_C or E_V.

As there is no charge in the oxide-semiconductor or metal-oxide interface or within the oxide and as the Fermi levels are equally spaced from vacuum levels, the energy bands are flat at equilibrium as shown in Fig. 5.24. The capacitance per unit area of the oxide is given by

$$C_{ox} = \frac{\grave{o}_{ox}}{t_{ox}} \text{ F/cm}^2 \qquad (5.20)$$

where,

$\grave{o}_{ox}$ - permittivity of oxide

t_{ox} - thickness of oxide

The capacitance of a MOS capacitor differ from that of a conventional capacitor. The capacitance value of MOS capacitor vary with bias applied to it. Under equilibrium condition, capacitance of ideal MOS capacitor is same as the capacitance of the oxide layer.

$$\text{i.e.,} \qquad C = C_{ox} = \frac{\grave{o}_{ox}}{t_{ox}} \qquad (5.21)$$

Band Bbending in MOS Devices

In MOS capacitor there is no current flow across the insulator from semiconductor to metal or metal to semiconductor under any bias. Therefore the Fermi level remain horizontal in the semiconductor because the current is proportional to the gradient in Fermi level. But a portion of the applied potential drops in the semiconductor near the oxide. Thus the presence of electric field in the semiconductor near the oxide causes bending of energy bands in the semiconductor. The energy bands bend upward in the direction of electric field, where electric field is present. This principle is used for drawing the energy band diagrams of MOS devices.

Accumulation ($V_G < 0$)

When a negative voltage is applied to the gate region, positive charges are induced on the semiconductor. These induced charges accumulate near the oxide semiconductor interface. The change in carrier concentration causes bending of energy bands at the interface. The distribution of charge density under this condition is shown in Fig. 5.25. As the induced charges are majority carriers they form a thin layer near the interface.

The semiconductor outside this accumulation region remains neutral and the energy band diagram is identical to the equilibrium energy band diagram in the neutral region. As the gate is

at negative potential, the Fermi level on the semiconductor side shifts down-ward by qV_G, where V_G is the applied gate voltage. Under this condition, the effective capacitance is the series combination of oxide capacitance and capacitance of accumulation layer. The capacitance of accumulation layer is very high as it is a very thin layer. Therefore, the effective capacitance under accumulation is same as C_{ox} (see equation 5.33 and Fig. 5.31).

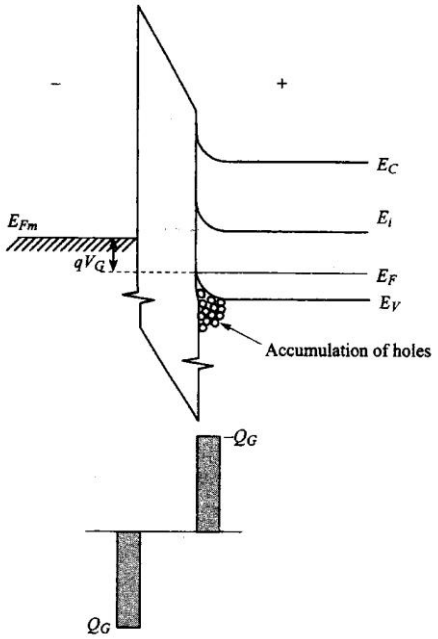


Fig. 5.25 Energy band diagram and distribution of charge density of ideal MOS capacitor under accumulation condition ($V_G < 0$)

Depletion ($V_G > 0$)

When a small positive gate voltage is applied, negative charges are induced in the p-type semiconductor. These negative charges recombine with holes in the semiconductor, which forms a region of immobile charges (depletion layer) near the interface. The energy band diagram and charge denisty distribution are shown in Fig. 5.26.

Notice the bending of energy bands indicating a decrease of hole concentration near the interface in the depletion layer. Now, the effective capacitance is the series combination of oxide capacitance and the depletion layer capacitance (C_D).

$$\text{i.e.,} \qquad C = \frac{C_{ox}C_D}{C_{ox} + C_D} \tag{5.22}$$

where, C - total capacitance / unit area
C_{ox} - oxide capacitance / unit area
C_D - depletion layer capacitance / unit area

The charge per unit area in the semiconductor in the depletion layer is given by

$$Q_s = -qN_AW \tag{5.23}$$

where, W - width of depletion layer

N_A - semiconductor doping concentration

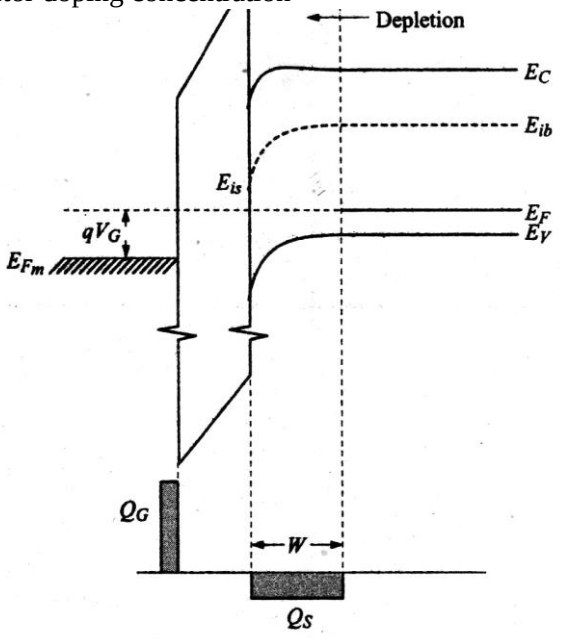


Fig. 5.26 Energy band diagram and distribution of charge density of an ideal MOS capacitor under depletion condition

Width of depletion layer is given by

$$W = \sqrt{\frac{2\grave{o}\phi_s}{qN_A}} \tag{5.24}$$

ϕ_s is called surface potential and is given by,

$$\phi_s = \frac{E_{ib} - E_{is}}{q} \tag{5.25}$$

where, E_{ib} - intrinsic level in the bulk

E_{is} - intrinsic level at the surface.

The capacitance decrease with increase in V_G as shown in Fig. 5.31.

Inversion

If V_G is increased further, the Fermi level on the semiconductor side moves up further. The bands bend down further so that the Fermi level at the surface lies above the intrinsic level. i.e., the surface gets inverted. This is because the induced electrons are attracted towards the surface and at the surface, the induced electron concentration exceeds hole concentration. The thin region in which the electron concentration exceeds hole concentration is called inversion layer.

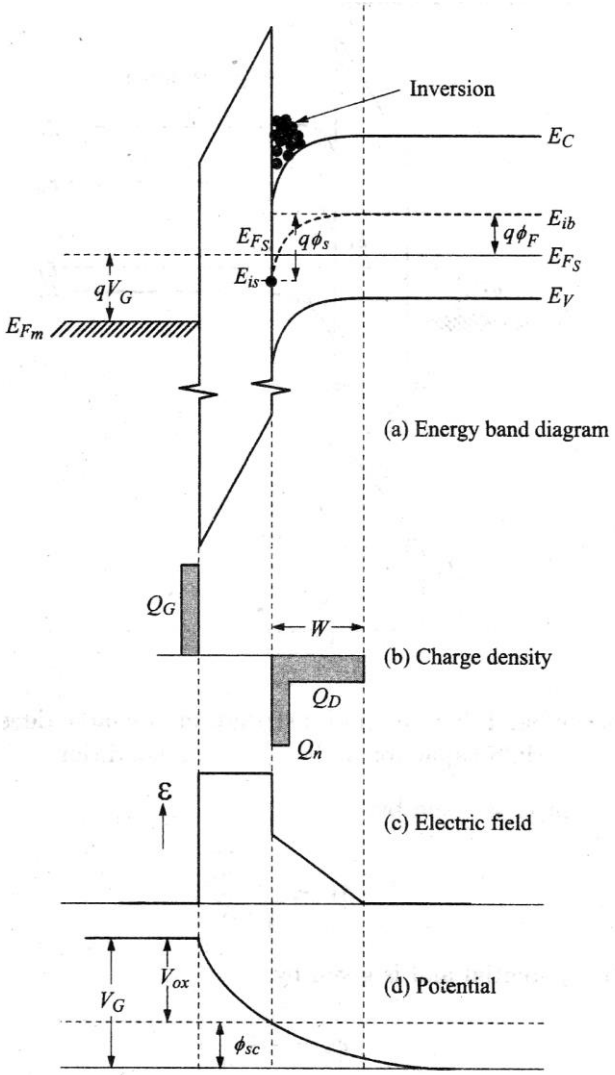


Fig. 5.27 MOS capacitor under inversion

Once inversion occurs at the surface, further increase in gate voltage can only increase inversion layer charge. The thickness of inversion layer is 50 to 100 A° and is very small compared to W. The total charge in the semiconductor under this condition is given by

$$Q_s = Q_n + Q_{Dm}$$

$$Q_s = Q_n - qN_A W \qquad (5.26)$$

where, Q_n - charge per unit area of electrons in the inversion layer

W_m - maximum width of depletion layer

Q_{Dm} - maximum value of the charge per unit area of depletion layer

On further increasing V_G, the intrinsic level at the surface goes below the Fermi level by an amount equal to that it is above the Fermi level at the bulk. Now, electron concentration at the surface become equal to hole concentration in the bulk. This condition is called strong inversion. Under strong inversion,

$E_F - E_{is} = E_{ib} - E_F$

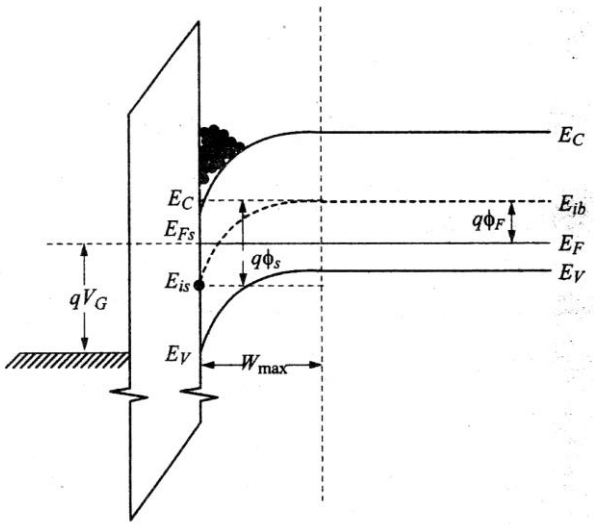


Fig. 5.28 Energy band diagram of MOS capacitor under strong inversion

The Fermi potential ϕ_F is defined by

$$q\phi_F = E_{ib} - E_F \qquad (5.27)$$

and it depends on the semiconductor doping.

The surface potential ϕ_s is defined by

$$q\phi_s = E_{ib} - E_{is} \qquad (5.28)$$

Under strong inversion,

$$E_F - E_{is} = E_{ib} - E_F$$

i.e, $E_{ib} - E_{is} = 2(E_{ib} - E_F)$

i.e., $\phi_s = 2\phi_F \qquad (5\text{-}29)$

Equation (5.29) shows that at strong inversion surface potential is twice Fermi potential.

Under strong inversion condition a conducting region (inversion layer of high electron concentration) is induced below the gate region.

Analytical Relation for Charge Densities

The hole and electron concentrations at equilibrium in a semiconductor is given by

$$p_0 = n_i e^{(E_{ib} - E_F)/kT}$$

$$= n_i e^{q\phi_F/kT} \cong N_A$$

$$n_0 = n_i e^{(E_F - E_{ib})/kT} = \frac{n_i^2}{p_0}$$

where $\phi_F = \frac{kT}{q} \ln \frac{N_A}{N_i}$, for p type semiconductor and $\phi_F = \frac{-kT}{q} \ln \frac{N_D}{n_i}$, for n type semiconductor.

The electron concentration at the surface of a p type semiconductor is given by

$$n_s = n_i e^{(E_F - E_{is})/kT}$$

$$= n_i e^{[(E_F - E_{ib}) + (E_{ib} - E_{is})]/kT}$$

$$= n_0 e^{q\phi_s/kT}$$

where $\phi_s = \frac{E_{ib} - E_{is}}{q}$ is called the surface potential.

Under thermal equilibrium

$\phi_s = 0 \qquad \therefore n(s) = n_0$

with increase in gate voltage ϕ_s increases which increases the electron concentration. When $\phi_s = \phi_F$; $n_0 = n_i$. This is the oneset of inversion. When ϕ_s exceeds, ϕ_F, the electron concentration at the surface n_s, exceeds n_i i.e., the surface of the semiconductor gets inverted. When $\phi_s = 2\phi_F$; $n_s = p_0 = N_A$. i.e., the minority carrier concentration at the surface equals the majority carrier concentration in the bulk. This condition is called strong inversion. The energy band diagram corresponding to the above situations are shown in Figures 5.24 to 5.28.

After strong inversion a small increase in V_G causes a large increase in n_s, so that the charges required to terminate the fields established by V_G are provided by the inversion region and not by an extension of the depletion region. Therefore depletion layer width remains almost constant after strong inversion.

5.3.2 C-V characterirtics of Ideal MOS System

The capacitance of MOS system vary with applied bias V_G. When a voltage V_G is applied to the gate, a part of it drops in the oxide and the remainder in semiconductor.

i.e., $V_G = V_{ox} + \phi_s$ (5.30)

But $V_{ox} = \frac{-Q_s}{C_{ox}}$

where Q_s is the charge on the semiconductor

$Q_s = -qN_AW + Q_n$

where Q_n is the inversion layer charge per unit area.

$\therefore \quad V_G = \frac{-Q_s}{C_{ox}} + \phi_s$ (5.31)

Differentiating equation (5.31) with respect to V_G

$$1 = \frac{1}{C_{ox}}\frac{dQ_s}{dV_G} + \frac{d\phi_s}{dQ_s}\frac{dQ_s}{dV_G} \tag{5.32}$$

Capacitance per unit area of the MOS system is defined by

$$C = \frac{dQ_G}{dV_G} = \frac{d(-Q_s)}{dV_G}$$

Semiconductor capacitance $C_S = \frac{-dQ_s}{d\phi_s}$

$\therefore$ Equation (5.32) becomes

$$1 = \frac{1}{C_{ox}}C + \frac{1}{C_s}C$$

i.e., $$\frac{1}{C} = \frac{1}{C_{ox}} + \frac{1}{C_s} \tag{5.33}$$

Equation (5.33) indicates that the oxide capacitance and semiconductor capacitance comes in series. Of these two capacitances C_{ox} is a constant for a particular MOS capacitor while C_s is dependent on bias.

At accumulation ($V_G < 0$) $C = C_{ox}$ and at depletion ($0 < V_G < V_{th}$), $C_S = C_D$, the depletion layer capacitance per unit area.

$$\therefore \quad C = \frac{C_D C_{ox}}{C_D + C_{ox}}$$

C_D decreases with increase in V_G due to the increase in depletion layer width. The depletion layer width reaches a maximum value under strong inversion. After that depletion layer capacitance remains constant.

A typical set up to measure the capacitance voltage (C-V) characteristics of MOS capacitor is shown in Fig. 5.29.

A dc bias (V_G) is applied to the MOS capacitor. The capacitance meter measures the capacitance by applying a small ac voltage (50 mV) on top of the dc bias and measuring the reactive current. By changing the dc bias using a ramp generator and plotting the capacitance as a function of dc bias, the C-V characteristics is obtained.

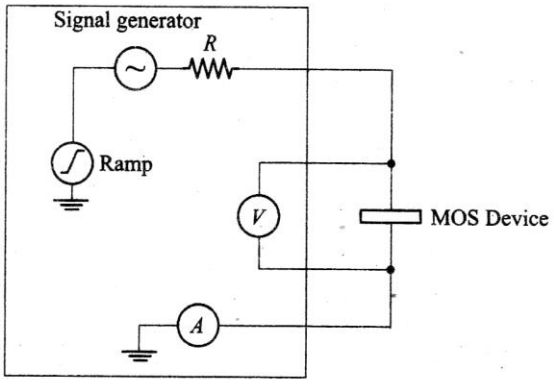
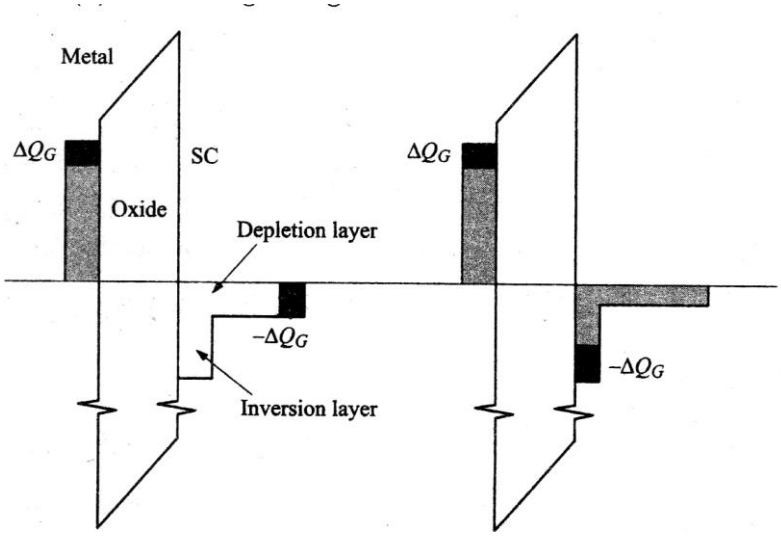


Fig. 5.29 Experimental setup to measure C-V characteristics of a MOS capacitor

If capacitance is measured with a high-frequency signal, the inversion layer cannot respond to the fast variation in the signal amplitude (see Fig. 5.30). The generation recombination time in the inversion layer is equal to the dielectric relaxation time (which is usually large). So, inversion layer has no capacitive effect. Therefore the depletion layer width adjusts itself to accomodate the variation in signal amplitude. As a result the effective capacitance remains constant at its minimum value, fixed by $C_{D(min)}$ as shown in Fig. 5.31 (b) on reaching strong inversion.

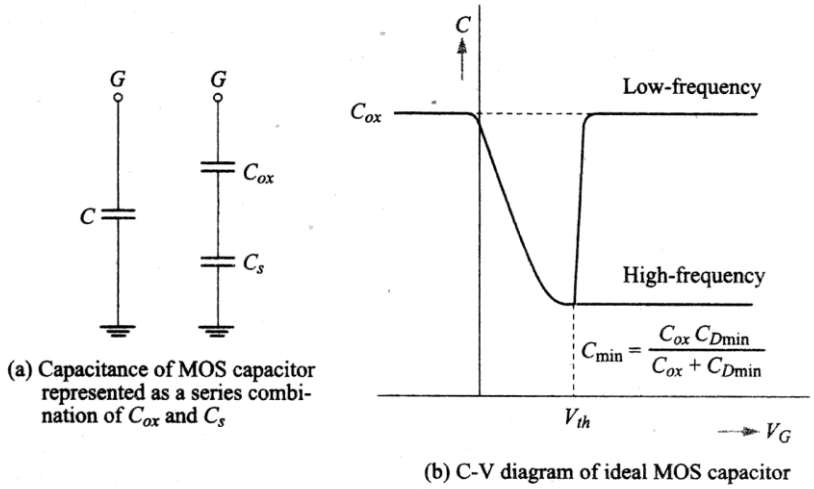


(a) At high-frequency the charge in inversion layer remains unchanged and the depletion layer charge changes

(b) At low-frequency, the depletion layer charge remains constant and inversion layer charge changes

Fig. 5.30 Effect of change in V_G on semiconductor charge. A change in gate voltage ΔV_G causes a corresponding change in charge ΔQ_G cm the metal side and $-\Delta Q_G$ on the semiconductor side

When capacitance is measured by super imposing low-frequency signal (~10 Hz), the inversion layer charge vary with the slow variation in signal amplitude. The depletion layer width remain unchanged and therefore the depletion layer capacitance is absent. The net capacitance is decided by inversion layer capacitance and oxide capacitance. Inversion layer capacitance is much greater than oxide capacitance (C_{ox}). Therefore, the effective capacitance is C_{ox}.



(a) Capacitance of MOS capacitor represented as a series combination of C_{ox} and C_s

(b) C-V diagram of ideal MOS capacitor

Fig. 5.31

Threshold Voltage

Threshold voltage is the voltage required to introduce strong inversion in the semiconductor. Under this condition a conducting 'n' layer is induced below the gate region.

$$V_{th} = V_{ox} + \phi_s$$

$$= \frac{-Q_s}{C_{ox}} + 2\phi_F$$

At the onset of inversion, $Q_s = Q_{Dm}$; $\phi_s = 2\phi_F$.

$$\therefore \quad V_{th} = \frac{-Q_{Dm}}{C_{ox}} + 2\phi_F \tag{5.34}$$

$$Q_{Dm} = \rho W_m$$

$$= -qN_A \, . \, W_m$$

$$W_m = \sqrt{\frac{2\grave{o}2\phi_F}{qN_A}}$$

$$\therefore \quad Q_{Dm} = -qN_A \sqrt{\frac{4\grave{o}\phi_F}{qN_A}} = \sqrt{4\grave{o}\phi_F qN_A}$$

$$V_{th} = 2\phi_F - \frac{\sqrt{4\grave{o}\phi_F qN_A}}{C_{ox}} \tag{5.35}$$

Example 5.4 For a MOS capacitor formed on p-type silicon substrate doped with $N_A = 5 \times 10^{16}$ cm^{-3}, determine the surface potential required to make the surface a. intrinsic b. at strong inversion.

Solution

a. $\phi_s = \phi_F = \frac{kT}{q} \ln \frac{N_A}{n_i} = 0.026 \ln \frac{5\times10^{16}}{1.5\times10^{10}}$

$= 0.391$ V

b. At strong inversion $\phi_s = 2\phi_F$

$= 2 \times 0.391$

$= 0.782$ V.

Example 5.5 A silicon MOS structure at 300 K is characterised by $N_A = 4 \times 10^{14}$ cm^{-3}, $t_{ox} = 0.1$ μm. Oxide is ideal. The metal is brought to a potential of +1 V with respect to semiconductor $\int_{rox} = 3.9$.

a. Does inversion occur?

b. Calculate voltage across oxide.

Solution

$$\phi_F = \frac{kT}{q} \ln \frac{N_A}{n_i} = 0.026 \ln \left(\frac{4\times10^{14}}{1.5\times10^{10}} \right) = 0.265 \text{ V}$$

$$W_m = \sqrt{\frac{4\grave{o}\phi_F}{qN_A}}$$

$$= \sqrt{\frac{4\times8.854\times10^{-14}\times11.8\times0.265}{1.6\times10^{-19}\times4\times10^{14}}}$$

$= 1.315 \times 10^{-4}$ cm

$Q_D = -qN_AW_m$

$= -1.6\times 10^{-19} \times 4 \times 10^{14} \times 1.315 \times 10^{-4}$

$= -8.416 \times 10^{-9}$ C/cm^2

$$C_{ox} = \frac{\in_{ox}}{t_{ox}}$$

$$= \frac{8.854\times10^{-14}\times3.9}{0.1\times10^{-4}} = 3.45 \times 10^{-8} \text{ F/cm}^2$$

$$V_{th} = \frac{-Q_D}{C_{ox}} + 2\phi_F$$

$$= \frac{8.416\times10^{-9}}{3.45\times10^{-8}} + 2 \times 0.265$$

$= 0.773$V

a. $V_{GS} = 1$ V. As $V_{GS} > V_{th}$ strong inversion occurs.

b. After strong inversion

$\phi_S = 2\phi_F$

$= 2 \times 0.265 = 0.53$ V

$V_{ox} = 1 - \phi_S$

$= 1 - 0.53$

$= 0.47$ V

Example 5.6 For Example 5.5 determine the capacitance of the MOS structure under biases of a. $V_{GS} = -1$ V, b. $V_{GS} = 1$ V.

Solution

a. $V_{GS} < 0$; accumulation

$$\therefore C = C_{ox} = 3.45 \times 10^{-8} \text{ F/cm}^2$$

b. $V_{GS} = 1$ V

$V_{GS} > V_{th}$; the structure is in. strong inversion mode; the capacitance depends on the frequency of the signal.

i. low-frequency

$C = C_{ox} = 3.45 \times 10^{-8}$ F/cm^2

ii. high-frequency

$$C = \frac{C_{ox}C_{D(\min)}}{C_{ox} + C_{D(\min)}}$$

$$C_{D(\min)} = \frac{\grave{o}_{si}}{W_m} = \frac{8.854\times10^{-14}\times11.8}{1.315\times16^{-4}} = 7.95 \times 10^{-9} \text{ F/cm}^2$$

$$C = \frac{3.45\times10^{-8}\times7.95\times10^{-9}}{\left(3.45\times10^{-8}+7.95\times10^{-9}\right)}$$

$= 6.46 \times 10^{-9}$ F/cm^2.

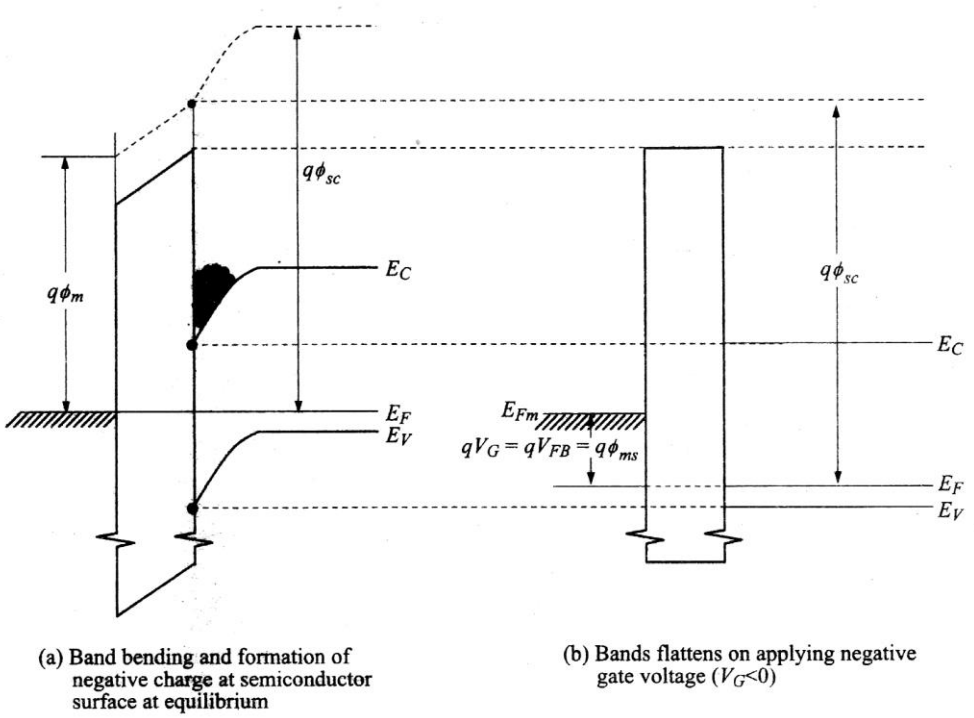
5.3.3 Real MOS Systems

In real MOS system (say Al, SiO_2, Si) work function of metal and semiconductor will be different. The charges at the interface (Si-SiO_2) and within the oxide must be taken into account.

Work Function Difference

Let ϕ_{ms} be the difference in work-function of metal and semiconductor.

$$\phi_{ms} = \phi_m - \phi_{sc}$$



(a) Band bending and formation of negative charge at semiconductor surface at equilibrium

(b) Bands flattens on applying negative gate voltage (V_G<0)

Fig. 5.32 Energy band diagram of a MOS capacitor with $\phi_{ms} < 0$

ϕ_{ms} is always negative for Al and Si. For negative ϕ_{ms}, an inversion layer may exist in the semiconductor under equilibrium as shown in Fig. 5.32(a). To obtain flat band condition a negative voltage must be applied to the gate ($V_{FB} = \phi_{ms}$) as shown in Fig. 5.32(b). The gate voltage required to obtain flat band condition is called flat band voltage.

Oxide, and Interface Charges

In addition to the work function difference, the equilibrium MOS structure is affected by charges in the insulator and oxide-semiconductor interface. The different types of charges in the oxide are shown in Fig. 5.33.

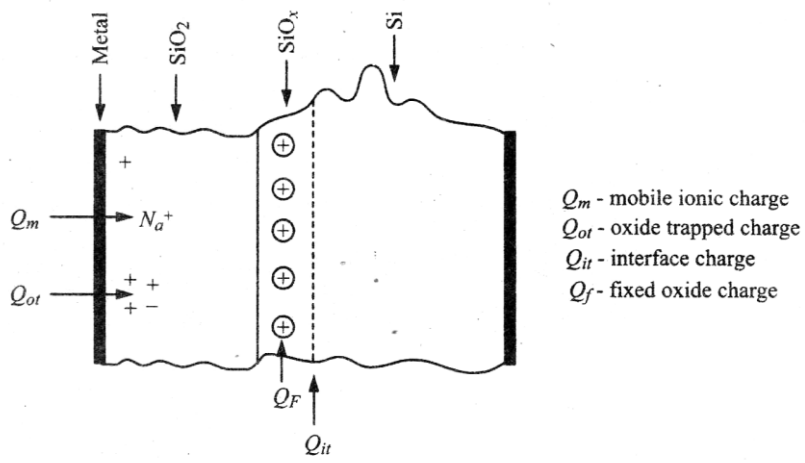


Fig. 5.33 Charges in a real oxide

Ionic charges Q_i) : Alkali ions such as Na^+ can move through crystalline SiO_2 which shifts the threshold voltage of MOS system.

Fixed oxide charges (Q_f) : These are charges located within the oxide as a sheet of positive charge near the Si-SiO_2 interface. These charges are formed during oxidation process.

Interface charges (Q_{it}) : These are charges present at the Si-SiO_2 interface due to the presence of dangling bonds due to sudden termination of semiconductor crystal lattice at the interface.

Oxide trapped charges (Q_{ot}) : The oxide may contain trapped charges within the defects present in the oxide. Holes are trapped within the oxide during processing whereas highly mobile electrons move away from the oxide. Therefore Q_{ot} is a positive charge.

The charges in the oxide layer will have a net positive sign and may be represented as Q_{ox}. This will induce an equivalent negative charge in the semiconductor. As a result the flat band voltage is shifted further by $\frac{Q_{ox}}{C_{ox}}$.

$$V_{FB} = \phi_{ms} - \frac{Q_{ox}}{C_{ox}} \tag{5.36}$$

Both terms bend the band downward. A negative voltage must be applied to the gate to obtain flat band condition.

Threshold Voltage

The voltage required to obtain flat band condition must be added to the threshold voltage of ideal MOS system to obtain the threshold voltage of real MOS system.

$$\therefore \quad V_{th} = V_{FB} - \frac{Q_{Dm}}{C_{ox}} + 2\phi_F$$

$$= \phi_{ms} - \frac{Q_{ox}}{C_{ox}} + \frac{Q_{Dm}}{C_{ox}} + 2\phi_F \tag{5.37}$$

Threshold voltage is the voltage required to induce a conducting layer (inversion layer) below the oxide. This includes the voltage required for flat band condition, the voltage to

accommodate the charge in the depletion layer and the voltage requried for strong inversion. Equation (5.37) is applicable to n-type and p-type substrates. The sign for different terms in the equation for n and p substrate are shown in Table 5.1.

Table 5.1 Sign of different terms in V_{th}

	ϕ_{ms}	$\frac{-Q_{ox}}{C_{ox}}$	$\frac{-Q_{Dm}}{C_{ox}}$	$+2\phi_F$
p-substrate (n-channel)	-ve	-ve	+ve	+ve
n-substrate (p-channel)	-ve	-ve	-ve	-ve

ϕ_{ms} and $\frac{-Q_{ox}}{C_{ox}}$ are negative for both p and n substrates. The last two terms are +ve for p-substrate (n-channel) and -ve for n-substrate (p-channel). Therefore V_{th} is always negative for p-channel device.

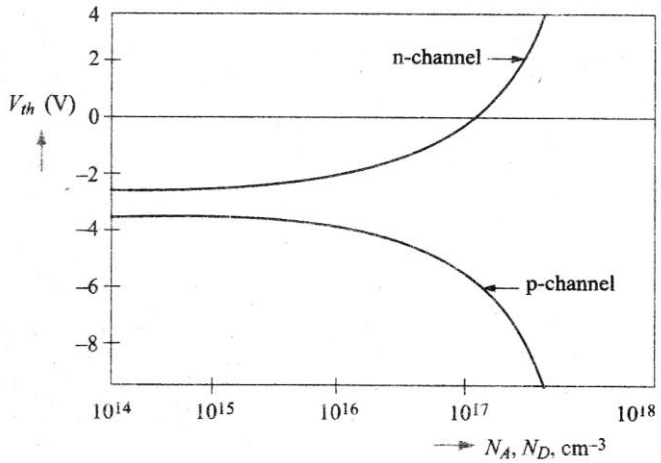


Fig. 5.34 Variation of threshold voltage with substrate doping for n-channel and p-channel MOS devices

For n-channel device V_{th} may be positive or negative. For low substrate doping the negative flat band voltage in the expression dominates and V_{th} is negative. With increase in doping $\frac{-Q_D}{C_{ox}}$ term increases and V_{th} becomes positive as shown in Fig. 5.34.

A p-channel MOS device will be ON only if $V_G < V_{th}$ and n channel device will be ON if $V_G > V_{th}$.

Polysilicon Gate

A heavily doped polysilicon shall be used in place of the gate metal. In this case the work function of the metal may be replaced by polysilicon work function. For heavily doped p-type (p^+) polysilicon E_F is at E_V and work function $q\phi_m = q\psi_s + E_g$. For n^+ polysilicon E_F is located at E_C.

$$\therefore \qquad q\phi_m = q\psi_s$$

where ψ_s represents semiconductor electron affinity.

Example 5.7 Determine flat band voltage and threshold voltage of a MOS device with p-type silicon substrate ($N_A = 10^{16}$ cm^{-3}) and Al as gate. Given $Q_{ox} = 5 \times 10^{10}$ qC/cm^2, $t_{ox} = 200$ Å, $\psi_s = 4.15$V, $\in_{rox} = 3.9$, $\phi_m = 4.2$ V, $E_g = 1.12$eV and $n_i = 1.5 \times 10^{10}$ cm^{-3}.

Solution

$$\phi_F = \frac{kT}{q} \ln \frac{N_A}{n_i}$$

$$= 0.026 \ln \frac{10^{16}}{1.5 \times 10^{10}} = 0.349 \text{ V}$$

$$\phi_{ms} = \phi_m - \left(\psi_s + \frac{E_g}{2q} + \phi F \right)$$

$$= 1.2 - \left(4.15 + \frac{1.12}{2} + 0.349 \right)$$

$$= -0.859 \text{ V}$$

$$Q_{Dm} = -qN_A W_m$$

$$W_m = \sqrt{\frac{4 \grave{o} \phi_F}{qN_A}}$$

$$= \sqrt{\frac{4 \times 8.854 \times 10^{-14} \times 11.8 \times 0.349}{1.6 \times 10^{-19} \times 10^{16}}} = 3.019 \times 10^{-5} \text{ cm}$$

$$Q_{Dm} = -1.6 \times 10^{-19} \times 10^{16} \times 3.019 \times 10^{-5}$$

$$= -4.83 \times 10^{-8} \text{ C/cm}^2$$

$$Q_{ox} = 5 \times 10^{10} \times 1.6 \times 10^{-19} = 8 \times 10^{-9} \text{ C/cm}^2$$

$$C_{ox} = \frac{\grave{o}_{ox}}{t_{ox}} = \frac{8.854 \times 10^{-14} \times 3.9}{200 \times 10^{-8}} = 1.726 \times 10^{-7} \text{ F/cm}^2$$

Flat band voltage $V_{FB} = \phi_{ms} - \frac{Q_{ox}}{C_{ox}}$

$$= -0.859 - \frac{8 \times 10^{-9}}{1.726 \times 10^{-7}}$$

$$= -0.905 \text{ V}$$

Threshold voltage $V_{th} = \phi_{ms} - \frac{Q_{ox}}{C_{oz}} + 2\phi_F - \frac{Q_{Dm}}{C_{oz}}$

$$= -0.859 - \frac{8 \times 10^{-9}}{1.726 \times 10^{-7}} + 2 \times 0.349 + \frac{4.83 \times 10^{-8}}{1.726 \times 10^{-7}}$$

= +0.072 V.

Example 5.8 Repeat Example 5.7 if $N_A = 5 \times 10^{17}$ cm^{-3}.

Solution

$$\phi_F = \frac{kT}{q} 1n \frac{N_A}{n_i}$$

$$= 0.0.261 1n \frac{5\times10^{17}}{1.5\times10^{10}} = 0.45V$$

$$\phi_{ms} = \phi_m - \left(\phi_s + \frac{E_g}{2q} + \phi_F \right)$$

$$= 4.2 - \left(4.15 + \frac{1.12}{2} + 0.45 \right) = -0.96V$$

$$Q_{D_m} = -qN_A W_m$$

$$W_m = \sqrt{\frac{4\times8.854\times10^{-14}\times11.8\times0.45}{1.6\times10^{-19}\times5\times10^{17}}}$$

$= 4.848 \times 10^{-6}$ cm

$$Q_{D_m} = -1.6\times10^{-19}\times5\times10^{17}\times4.848\times10^{-6}$$

$= -3.878 \times 10^{-7}$ C/cm^2

$$Q_{ox} = 8\times10^{-9} C/cm^2$$

$$C_{ox} = 1.726\times10^{-7} F/cm^2$$

$$V_{FB} = \phi_{ms} - \frac{Q_{ox}}{C_{oz}}$$

$$= -0.96 - \frac{8\times10^{-9}}{1.726\times10^{-7}} = 1.006V$$

$$V_{th} = \phi_{ms} - \frac{Q_{ox}}{C_{oz}} - \frac{Q_{D_m}}{C_{oz}} + 2\phi F$$

$$= -0.96 \frac{8\times10^{-9}}{1.726\times10^{-7}} + \frac{3.878\times10^{-7}}{1.726\times10^{-7}} + 2\times0.45$$

= 2.141 V.

Example 5.9 Repeat Example 5.8 if t_{ox} 300 A

Solution

$\phi_F = 0.45$ V

$\phi_{ms} = -0.96$ V

$W_m = 4.848 \times 10^{-6}$ cm

$Q_{Dm} = -3.878 \times 10^{-7}$ C/cm^2

$Q_{ox} = 8 \times 10^{-9}$ C/cm^2

$$C_{ox} = \frac{\in_{ox}}{t_{ox}} = \frac{8.854 \text{ x } 10^{-14} \text{ x } 3.9}{300 \text{ x } 10^{-8}} = 1.151 \times 10^{-7} \, F / cm^2$$

$$V_{FB} = \phi_{ms} - \frac{Q_{ox}}{C_{ox}} = -0.96 - \frac{8 \text{ x } 10^{-9}}{1.151 \text{ x } 10^{-7}} = -1.0295 \, V$$

$$V_{th} = \phi_{ms} - \frac{Q_{ox}}{C_{ox}} - \frac{Q_{D_m}}{C_{ox}} + 2\phi_F$$

$$= -0.96 - \frac{8 \text{ x } 10^{-9} \text{ x } 3.9}{1.151 \text{ x } 10^{-7}} + \frac{3.878 \text{ x } 10^{-7} \text{ x } 3.9}{1.151 \text{ x } 10^{-7}} + 2 \times 0.45$$

= 3.2395 V.

The above results show that an increase in t_{ox} and N_A increase V_{th}. This principle is used for isolation in MOSFETs.

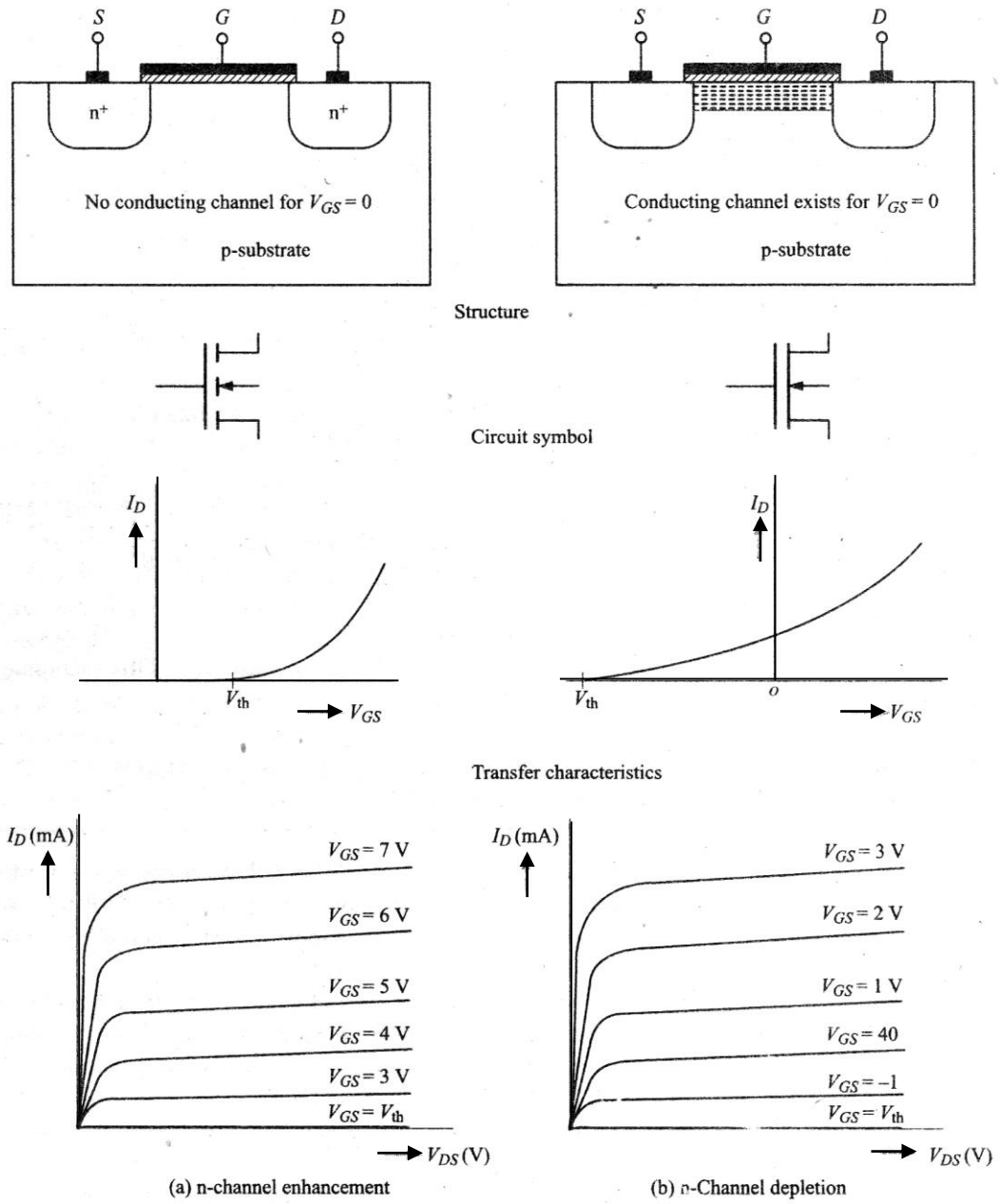
5.4 METAL OXIDE SEMICONDUCTOR FIELD EFFECT TRANSISTOR (MOSFET)

MOSFET makes use of a MOS structure to realize field effect. Low power consumption and less area of occupancy makes MOSFET a better choice than BJT for VLSI circuits. They are used extensively in fabrication of computer memory, digital signal processors and many other applications.

Depending on the substrate type, MOSFET can be n-channel (n-MOS) or p-channel (p-MOS). The substrate for n-MOS is p-type and for p-MOS is n-type. An n-channel MOSFET has higher speed and better high-frequency response with the same geometry and dimension. This is due to higher mobility of electrons. Our discussion is limited to n-channel MOSFETs. But the results are valid for a p-channel device also with appropriate modifications.

MOSFETs may be further classified as enhancement type and depletion type on the basis of operating mode. Enhancement type MOSFET is normally OFF. No channel exists for VGS = 0 and no current flows between source and drain when gate voltage is zero. The channel is induced by a positive gate voltage. Depletion type MOSFETs are usually ON. A conducting channel exists for VGS = 0. The device is turned OFF by depleting the channel by applying a negative gate voltage.

The simplified structure and characteristics of n-channel enhancement and depletion MOSFETs are shown in Fig. 5.35.



Drain characteristics

Fig. 5.35 Simplified structure, citcuit symbol, transfer characteristics and drain characteristics of MOSFET

In enhancement MOSFET a positive gate voltage greater than threshold voltage (V_{th}) has to be applied to induce conducting channel. On further increase of gate voltage, channel conductance increases. The drain current also increases. The conductance of channel is enhanced by the voltage applied to the gate.

In depletion MOSFET the substrate is lightly doped so that the threshold voltage is negative. In this case, ϕ_{ms} and the positive charges in the oxide induce an inversion layer in the channel without applying a gate voltage. This induced channel can be removed only by applying a negative gate voltage. The depletion MOSFET can be turned off by applying a negative gate voltage with magnitude greater than V_{th}.

5.4.2Principle of Operation

Principle of operation of n-channel enhancement MOSFET is as follows:
Cut-off region: With $V_{GS} < V_{th}$ conducting channel does not exist. Current between drain and source is zero. Under this condition for any value of V_{DS}, the structure between drain and source consists of two reverse-biased diodes connected back-to-back and current is zero.

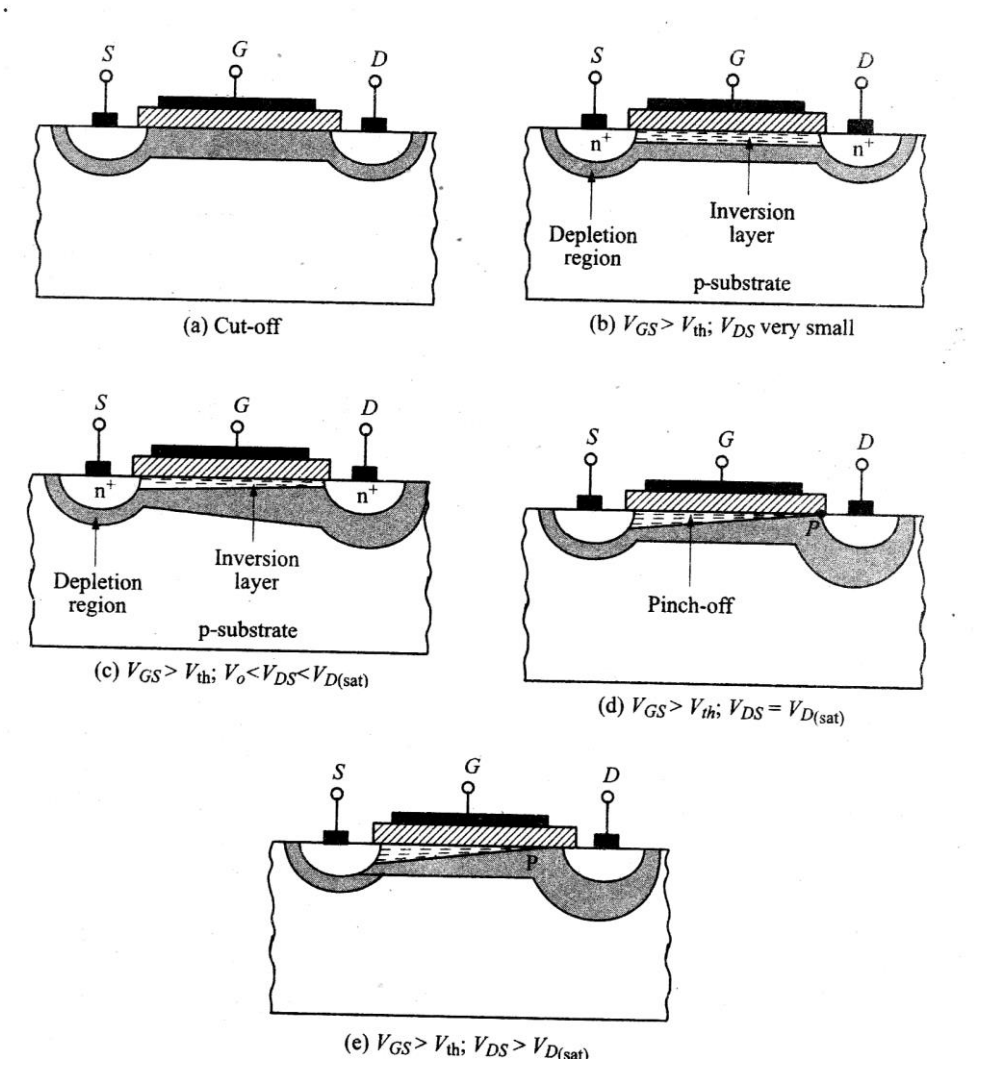
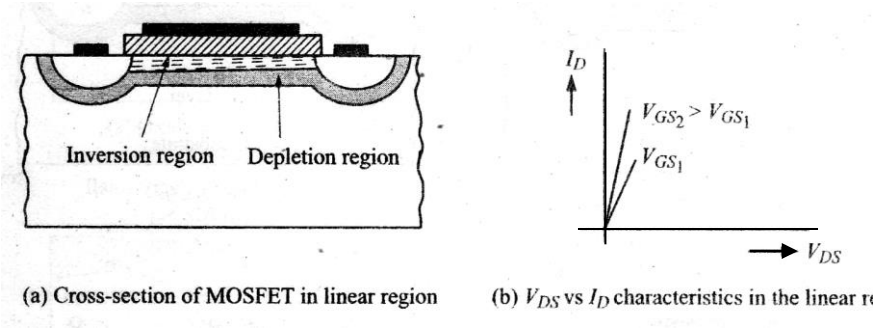


Fig. 5.37 Cross-section of n-channel MOSFET under various bias conditions

Linear region: In this region voltage applied to the gate is greater than V_{th}, so that a conducting channel exists between source and drain regions. A depletion layer also exist as in the case of a JFET as shown in Fig. 5.38(a).

For small values of drain to source voltage (hundreds of milli volts), the conductance of the channel remains constant Fig. 5.37(b). For a fixed V_{GS} the channel acts as a simple resistance and drain current increases linearly with increase in V_{DS}. With increase in V_{GS} (towards positive) the conductance of channel increases due to increase in inversion layer charges and the slope of the drain characteristics increases as shown in Fig. 5.38(b).

As V_{DS} is increased further the depletion layer charge increases, which results in decrease of the inversion layer charge (for a given V_{GS} the net charge on the semiconductor side remains constant). As the reverse-bias is more near the drain end of the channel, the channel has a shape as shown in Fig. 5.37(c). The effective resistance of channel increases, causing a reduction in slope of characteristics.



(a) Cross-section of MOSFET in linear region (b) V_{DS} vs I_D characteristics in the linear r

Fig. 5.38

Saturation region: As V_{DS} is increased further the channel gets pinched-off at the drain end, i.e., the inversion layer thickness reduces to zero as shown in Fig. 5.37(d). The inversion layer charge at the drain end becomes zero. The drain current saturates at this value of V_{DS}. As in the case of JFET further increase in V_{DS} do not produce any increase in drain current as the inversion layer charge remain almost constant (Fig. 5.37(e)). Complete characteristics is shown in Fig. 5.35(a).

In the case of depletion MOSFETs, a conducting channel exists for $V_{GS} = 0$. The conductance of channel increases with increase in V_{GS}. Channel can be depleted by applying a negative gate voltage. The minimum negative gate voltage required to deplete the channel is called threshold voltage (Mathematical expressions for threshold voltages are exactly same as those for MOS capacitors). The characteristics of n-channel depletion MOSFET is shown in Fig. 5.35(b).

5.4.3 I-V Characteristics (Derivation)

The structure used for this derivation is shown in Fig. 5.39. The derivation is based on the following approximations.

(1) The current flow through the channel is one dimensional. No current flows between source and gate.

(2) The electron mobility in the channel is constant,.

(3) The source and substrate are grounded.

(4) The depletion layer charge density remains constant from source to drain.

(5) The potential, gradient from drain to source is much smaller than that from gate to channel. Therefore, the electron density in the channel is decided by the gate to channel potential. This approximation is known as gradual channel approximation.

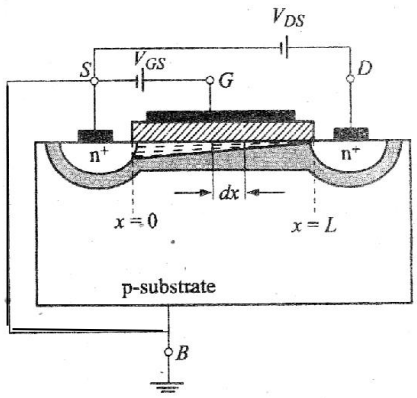


Fig. 5.39 Structure of an n-channel MOSFET

The expression for drain current I_D is derived by expressing the electron density in the channel (inversion layer) as a function of distance from source. A part of the voltage applied between gate and source flattens the band and the remaining voltage drops across the oxide and semiconductor.

i.e $$V_G = V_{ox} + \phi_s + V_{FB} \tag{5.38}$$

where $V_{ox} = \dfrac{-Q_s}{C_{ox}}$

ϕ_s = voltage at the surface of semiconductor

$V_{FB} = \phi_{ms} - \dfrac{Q_{ox}}{C_{ox}}$

At strong inversion the voltage at the surface of the semiconductor

$$\phi_s = 2\phi_F + V(x)$$

where V(x) is the potential drop in the channel at distance x from the source.

Therefore equation (5.38) may be written as

$$V_G = \frac{-Q_s}{C_{ox}} + 2\phi_F + V_{FB} + V(x) \tag{5.39}$$

Q_s represents the charge in semiconductor and is given by

$$Q_s = Q_n(x) + Q_D(x) \tag{5.40}$$

Q_n - inversion layer charge

Q_D - charge in depletion layer

$$Q_D = \sqrt{2\grave{o}qN_A(2\phi_F + V(x))}$$

In this derivation Q_D is assumed to be independent of $V_{(x)}$; i.e., $Q_D = \sqrt{4\grave{o}qN_A\phi_F}$

Substituting for Q(s) from equation (5.40) in equation (5.39),

$$V_{GS} = \frac{-(Q_n(x)Q_D(x))}{C_{ox}} + 2\phi_F + V_{FB} + V(x)$$

$$Q_n(x) = C_{ox}\left[V_{GS} - V_{FB} - 2\phi_F - V(x)\right] - Q_{D(x)}$$

$$= -C_{ox}\left[V_{GS} - V(x) - \left(V_{FB} + 2\phi_F - \frac{Q_D(x)}{C_{ox}}\right)\right] \quad (5.41a)$$

$$= -C_{ox}\left[V_{GS} - V(x) - V_{th}\right] \quad (5.41b)$$

Resistance of a differential length dx at distance x from the source is given by

$$dR = \frac{-dx}{Q_n(x)\bar{\mu}_n Z}$$

where, $\bar{\mu}_n$ - effective surface mobility of channel

Z - width of the channel.

Since, the current through the channel is constant, the voltage drop dV(x) in a differential resistance dR of a differential length dx of channel is given by

$$dV(x) = I_D.dR$$

$$= \frac{-I_D.dR}{Z\bar{\mu}_n Q_n(x)}$$

Substituting the value of $Q_n(x)$ from equation (5.41)

$$dV(x) = \frac{-I_D.dx}{Z\bar{\mu}_n(-C_{ox})\left[V_{GS} - V(x) - V_{th}\right]}$$

$$I_D.dx = \bar{\mu}_n C_{ox} Z\left[V_{GS} - V(x) - V_{th}\right]dV(x) \quad (5.42)$$

Integrating the above equation from source end to drain end of the channel,

$$\int_0^L I_D.dx = \bar{\mu}_n C_{ox} Z \int_0^{V_{DS}} \left[V_{GS} - V(x) - V_{th}\right]dV(x)$$

$$I_D = \bar{\mu}_n C_{ox} \frac{Z}{L}\left[(V_{GS} - V_{th})V_{DS} - \frac{V_{DS}^2}{2}\right] \quad (5.43)$$

Equation (5.43) does not take into account the increase in depletion layer charge as we move from source to drain. Due to increase in Q_D, Q_n decreases and resistance increases from source to drain. As a result the actual drain current will be less than that given by equation (5.43). The equation is valid only if the channel exists from source to drain.

Q_n at drain end become zero when $V_{DS} = V_{D(sat)}$

$$V_{DS} = V_{D(sat)} = V_{GS} - V_{th}$$

Therefore as long as $V_{DS} \geq V_{D(sat)}$ equation (5.43) reduces to

$$I_{D(sat)} = \bar{\mu}_n C_{ox} \frac{Z}{L}\left[(V_{GS} - V_{th})(V_{GS} - V_{th}) - \frac{(V_{GS} - V_{th})^2}{2}\right]$$

$$= \bar{\mu}_n C_{ox} \frac{Z}{2L}(V_{GS} - V_{th})^2$$

$$= \frac{k_P}{2}(V_{GS} - V_{th})^2$$

where k_p is a device parameter given by

$$k_P = \bar{\mu}_n C_{ox} \frac{Z}{L}$$

If $V_{GS} > V_{th}$ and $V_{DS} \leq V_{GS} - V_{th}$

$$I_D = k_p \left[(V_{GS} - V_{th}) V_{DS} - \frac{V_{DS}^2}{2} \right] \quad (5.44)$$

If $V_{GS} \geq V_{th}$ and $V_{DS} \geq V_{GS} - V_{th}$

$$I_D = \frac{k_p}{2}(V_{GS} - V_{th})^2 \quad (5.45)$$

If $V_{GS} < V_{th}$

$I_D = 0$

The I-V relationship represented by equations (5.44) and (5.45) is called square law model

5.4.4 Real MOSFET

The MOSFET we have discussed so far is an ideal MOSFET which does not take into account the secondary effects such as channel length modulation, substrate bias, temperature dependence etc.

Effect of Variation of Depletion Layer Charge

The square law model neglects the variation of depletion layer charge along the channel. It under-estimates the depletion layer width and over-estimates the inversion layer charge density. Current given by square law model is much greater than the actual current.
To account for the charge variation in depletion layer, Q_D in the square law model has to be replaced by $\sqrt{2\grave{o}qN_A(q\phi_F + V(x))}$. . The resulting expression for drain current is called bulk charge model, which is a better approximation to MOSFET currents than square law model.

Effective Mobility

Mobility is defined as the ratio of average drift velocity to electric field. In a semiconductor, mobility is usually limited by lattice scattering and ionised impurity scattering. But in MOSFETs the charge carriers are restricted to an extremely thin layer between the oxide and bulk of the semiconductor- The carrier mobility is affected by transverse electric field due to gate voltage. The carriers are forced to bounce between the oxide and bulk of the semicondcufcor.Therefore, the mobility of carriers is considerably reduced. Depending on the gate voltage, effective mobility in the channel of MOSFET $(\bar{\mu}_n)$ may vary between 30 to 50% of bulk mobility.

Effect of Substrate Bias

In MOSFET, the substrate is either shorted to source or given a reverse-bias with respect to source. In n-channel MOSFET (p-type substrate), substrate is either grounded or connected to a negative potential with respect to source. The voltage applied to the substrate is also called body voltage (V_B). With a reverse-bias at substrate, the depletion layer will be more, and more band bending is required for flat band condition. Therefore the gate voltage required for inversion of channel (V_{th}) increases with increased reverse bias to the substrate. The increase in threshold voltage with reverse-bias applied to body is known as body effect.

In the case of p-channel MOSFETs, threshold voltage become more negative with increase in substrate reverse-bias. Change in threshold voltage due to substrate bias V_B may be expressed as

$$\Delta V_{th} = \gamma\sqrt{|2\phi_F| - |V_{SB}|} - \sqrt{|2\phi_F|} \tag{5.46}$$

where γ is called body factor and is given by

$$\gamma = \frac{\sqrt{2\grave{o}qN_A}}{C_{ox}} \tag{5.47}$$

Sub Threshold Conduction

For $|V_{GS}| < |V_{th}|$ a MOSFET is assumed to be OFF and the current to be zero. But actually conduction in MOSFETs starts well before strong inversion. This is known as sub threshold or weak inversion conduction. In the weak inversion region, the current in MOSFET can be approximated as that in a BJT formed by n^+ source (emitter) p-substrate (base) and n^+ drain (collector) and as given by eqn 5.48.

$$I_D = I_S e^{(V_{GS}/nV_T)}(1 - e^{(-V_{DS}/nV_T)})(1 + \lambda V_{DS}) \tag{5.48}$$

where n is a constant lying between 1 and 2. In the sub threshold region ($V_{GS}<V_{th}$), the drain current increases exponentially with V_{GS} as given by eqn 5.48 and shown in Fig. 5.40. For low power applications MOSFETs can be operated in sub-threshold region with low supply voltage.

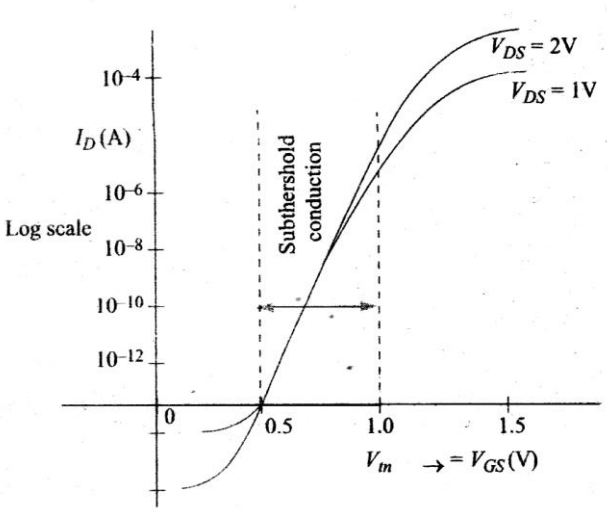


Fig.5.40

Channel Length Modulation

After pinch-off, if V_{DS} is increased further, the effective length of channel decrease due to depletion of channel as shown in Fig. 5.41. The voltage in excess of $V_{D(sat)}$ drops in the depleted portion and $V_{D(sat)}$ drops in the conducting channel. As represented by the current equation, the current is inversly proportional to channel length L. Therefore as V_{DS} increases beyond V_{DSsat}, the effective length of the channel L decreases, say by (ΔL) and I_D increases. This effect is negligible in long channel devices. But in modern short channel high speed devices, ΔL is not negligible and the drain current increases with increase in V_{DS} and is called channel length modulation. This is similar to base width modulation in BJT.
The channel length modulation can be incorporated in square law model, so that equation (5.45) becomes

$$I_{D(sat)} = \frac{k_p}{2}(V_G - V_{th})^2(1+\lambda V_{DS}) \qquad (5.49)$$

where the channel length modulation parameter (λ_p) varies between 0.01 V^{-1} to 0.02 V^{-1}.

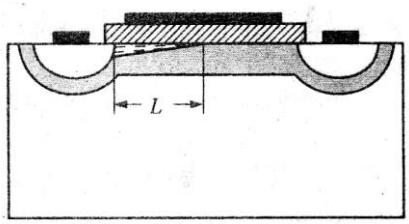


Fig. 5.41 Channel length modulation (as V_{DS} exceeds $V_{D(sat)}$ the effective length of the channel decreases)

Fig. 5.42 shows the effect of channel length modulation on the drain characteristics.

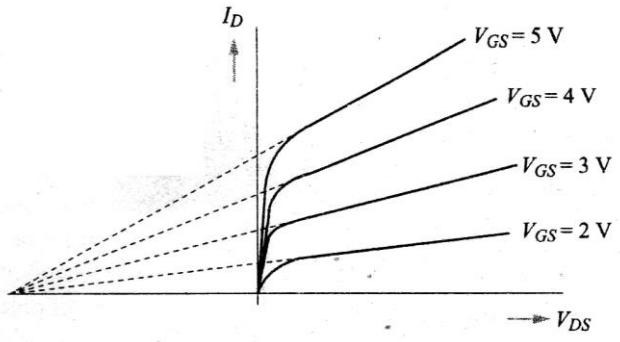


Fig. 5.42 Effect of channel length modulation on drain characteristics

Drain Induced Barrier Lowering

In MOSFETs when a voltage is applied to the gate, the channel is initially depleted and inversion starts after that. The depletion layers towards the channel side of the source channel and drain channel p-n junctions deplete a part of the channel. As channel length reduces, the percentage of the channel depleted by these pn junctions increases. As a result the gate voltage required to deplete the channel decrease, leading to a reduction in threshold voltages.

As V_{DS} increases the depletion layer widths of the p-n junctions increases, leading to a reduction in threshold voltage. This phenomenon is known as drain induced barrier lowering (DIBL). At higher V_{DS}, the drain and source may get shorted, which is known as punch through. Due to DIBL the threshold voltage decreases with reduction in channel length and increase in drain to source voltage.

Velocity Saturation

In conventional MOSFETs (long channel) velocity of charge carriers do not saturate when current saturate. But in short channel MOSFETs (channel length less than a micrometer), the velocity of charge carriers saturate at a V_{DS}, less than that required for pinch off, leading to saturation of current at a lower value of V_{DS}. This is due to the high electric field present in the channel $\mathrm{E} = \frac{V_{DS}}{L}$. At high electric field, velocity of charge carriers saturate as explained in section 1.12.

The MOSFET current in the saturation region, with velocity saturation may be modeled as

$$I_{D(sat)} = WC_{ox}(V_{GS} - V_{th})v_{sat}$$

where v_{sat} represents the saturation velocity of electron $v_{sat}=10^7$ cm/s for electrons in silicon at 300 K) and W, the width of the channel. The two effects of velocity saturation are:

(i) I_{Dsat} for a given V_{GS} reduces significantly.

(ii) The current in the saturation region depends linearly on V_{GS} in contrast to the square law dependence in long channel devices.

The characteristics of MOSFET without and with effects of velocity saturation are shown in Fig. 5.43.

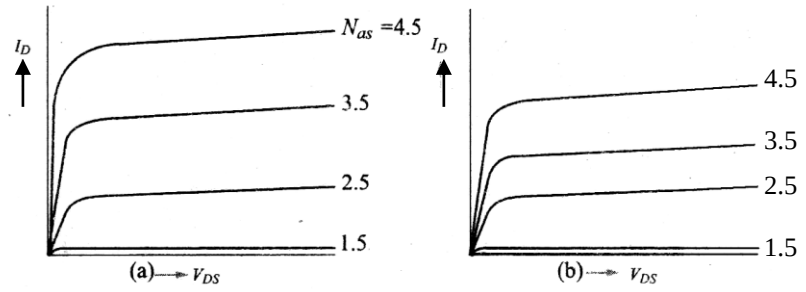


Fig. 5.43 Drain characteristics of MOSFET (a) without velocity saturation (b) with velocity saturation

Hot Electron Effect

A hot electron is an electron with high kinetic energy. In short channel devices electrons become hot at normal operating voltages. Electric field of the order of 10^4V/cm is required for this. The hot electrons moving from source to drain of channel penetrate into the gate oxide,

leading to an increase in threshold voltage. The gradual migration of hot electrons into the gate oxide, on extensive usage lead to reduction in drain current and the device may remain OFF permanently, limiting the life of the circuit. Lightly doped drain (LDD) structure reduces this effect. The peak electric field in the channel can be reduced by reducing the source and drain doping near the channel.

Temperature Dependence

The effect of change in temperature on MOSFET characteristics is much less than that in BJT characteristics.

Increase in temperature reduces threshold voltage due to reduction in ϕ_F. This results in an increase of drain current. But with increase in temperature the mobility reduces due to increased lattice scattering causing reduction in drain current. At low currents effect of increase in temperature on V_T is more dominant and increase of temperature increases drain current. At high currents effect of reduction in mobility by lattice scattering is dominant and drain current decreases with increase in temperature.

Handling of MOSFET (electrostatic discharge)

The thickness of oxide in MOSFET is very small (several A°). So, the dielectric breakdown voltage of the gate oxide is small, E_{crit} *of* SiO_2 ; 2×10^7V/cm. For t_{0x} = 50 A°, the gate voltage that results in breakdown of channel is 10V only.

The static voltage developed in human body may damage MOSFET just on touching it. Touching the gate of MOSFET causes discharge of static voltage through it, and immediate destruction of MOSFET. Before touching MOSFET, static electricity accumulated in human body must be discharged by touching the work bench.

Example 5.10 A silicon n-channel MOSFET with n^+ polysilicon gate has N_A=5x10^{16} cm^{-3}, Q_{ox}=5×10^{10} qC/cm^2, t_{ox} = 300 A, $\bar{\mu}_n$ = 600 cm^2/V_S, Z = 50 μm, L = 10 μm, ε_{rox}=3.9 and E_g =1.11 eV. Using square law model, calculate the drain current at

a. V_{GS} = +2 V, V_{DS} = 1 V

b. V_{GS} = +3 V, V_{DS} = 5 V

Solution

$$V_{th} = \phi_{ms} - \frac{Q_{ox}}{C_{ox}} - \frac{Q_{DM}}{C_{ox}} + 2\phi_F$$

$$\phi_F = \frac{kT}{q} 1n \frac{N_A}{n_i}$$

$$= 0.0261n \frac{5\times10^{16}}{1.5\times10^{10}} = 0.30V$$

$$\frac{(E_C - E_F)}{q}_{substrate} = \frac{E_g}{2q} + \phi_F = 0.55 + 0.39 = 0.04V$$

$$\phi_{ms} = \frac{E_C - E_F}{q}_{poly} - \frac{E_C - E_F}{q}_{substrate}$$

$$= 0 - 0.94 = -0.94 \text{ V}$$

$$C_{ox} = \frac{E_{ox}}{t_{ox}}$$

$$= \frac{8.854 \times 10^{14} \times 3.9}{300 \times 10^{-8}} = 1.15 \times 10^{-7} F / cm^2$$

$$Q_{Dm} = -qN_A W_m$$

$$W_m = \sqrt{\frac{4\grave{o}\phi_F}{qN_A}}$$

$$= \sqrt{\frac{4 \times 8.854 \times 10^{-14} \times 11.8 \times 0.39}{1.6 \times 10^{-16} \times 5 \times 10^{16}}}$$

$$= 1.427 \times 10^{-5} \text{ cm}$$

Q_{Dm} $= 1.6 \times 10^{-19} \times 5 \times 10^{16} \times 1.427 \times 10^{-5}$

$= -1.142 \times 10^{-7}$ C/cm^2

V_{th} $= -0.94 - \frac{5 \times 10^{10} \times 1.6 \times 10^{-19}}{1.15 \times 10^{-7}}$

$+ \frac{1.142 \times 10^{-7}}{1.15 \times 10^{-7}} + 2 \times 0.39$

$= 0.763$ V

V_{GS} $= +2$ V

V_{DS} $= 1$ V

$V_{D(sat)}$ $= V_{GS} - V_{th}$

$= 2 - 0763 = 1.237$ V

$V_{DS} < V_{D(sat)}$. Therefore MOSFET is in linear region..

$$I_D = k_p \left[(V_{GS} - V_{th}) V_{DS} - \frac{V_{DS}^2}{2} \right]$$

$$k_p = \frac{\bar{\mu}_n C_{ox} Z}{L}$$

$$= \frac{600 \text{ x } 1.15\text{x } 10^{-7} \text{ x } 50 \text{ x } 10^{-4}}{10 \text{ x } 10^{-4}} \text{ 10 x 10-4}$$

$$I_D = 3.45 \times 10^{-4} \left[(2 - 0.763) 1 - \frac{1^2}{2} \right]$$

$= 0.254$ mA

b. V_{GS} $= +3$V, $V_{DS} = 5$V

$V_{D(sat)} = 3 - 0.763 = 2.237$ V

$V_{DS} > V_{D(sat)}$

Therefore MOSFET is in saturation region.

$$I_{D(sat)} = \frac{k_p}{2}(V_{GS} - V_{th})^2$$

$$= \frac{3.45\times10^{-4}}{2}(3-0.763)^2$$

$= 0.863$ mA.

Example 5.11 For the MOSFET discussed in Example 5.10, determine the saturation current at $V_{GS} = 4$ V and a. $V_{DS} = 3.6$ V b. $V_{DS} = 5$ V c. $V_{DS}=10$V. Consider the channel length modulation parameter $\lambda_p = 0.02\ V^{-1}$.

Solution

$V_{th} = 0.763$ V, $k_p = 3.45 \times 10^{-4}$

$V_{DS} = 3.6$V, $V_{GD} = 4$V

a. $V_{D(sat)} = V_{GS} - V_{th}$

$= 4-0.763 = 3.237$ V, $V_{DS} > V_{D(sat)}$

$$V_{D(sat)} = \frac{k_p}{2}(V_{GS} - V_{th})^2(1+\lambda_p V_{DS})$$

$$= \frac{3.45\times10^{-4}}{2}(4-0.763)^2(1+0.02\times3.6)$$

$= 1.937$mA

b. $V_{DS} = 5$V

$$I_{D(sat)} = \frac{3.45\times10^{-4}}{2}(4-0.763)^2(1+0.02\times5)$$

$= 1.988$ mA

c. $V_{DS} = 10$V

$$I_{D(sat)} = \frac{3.45\times10^{-4}}{2}(4-0.763)^2(1+0.02\times10)$$

$= 2.169$ mA.

Control of Threshold Voltage

MOSFETs in digital applications generally require positive threshold voltage (i.e., they are normally OFF).

For that $\frac{-Q_D}{C_{ox}} + 2\phi_F > V_{FB}$

Threshold voltage can be increased by

(1) Increasing the oxide thickness: But this will reduce the transconductance and voltage gain of MOSFET.

(2) Increasing channel doping: Increase in channel doping increases the depletion layer charge density and therefore the threshold voltage. But this increases the substrate capacitance and reduces the breakdown voltage. Large doping concentration also reduces mobility.

In practical MOSFETs the threshold voltage may be different from that given by equation (5.37) due to variation in mobility, oxide thickness and oxide charges. Therefore a method known as threshold tailoring implant is done to adjust the threshold voltage during fabrication. In n-channel device Boron is ion implanted into the channel region to control threshold voltage. This method enables precise control of voltage. It also allows the fabrication of MOSFETs with different threshold voltages on the same wafer.

The change in flat band and threshold voltages due to the implantation of charge Q_I/cm^2 in the oxide, at a distance x from the metal is

$$\Delta V_{FB} = \Delta V_{th} = \frac{-Q_I}{\left(\frac{\epsilon_{ox}}{x}\right)} = \frac{-Q_I x}{\epsilon_{ox}}$$

(This is equivalent to the voltage required to charge a capacitor of value $\frac{\epsilon_{ox}}{x}$ to the charge - Q_I.)

$$\Delta V_{FB} = \frac{-Q_I x}{\epsilon_{ox}}$$

$$= \frac{-Q_I x}{C_{ox} t_{ox}} \quad \left(\text{Q} \quad C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}\right) \tag{5.50a}$$

If the impurities are implanted at the oxide semiconductor interface

$$\Delta V_{FB} = \frac{-Q_I}{C_{ox}} \tag{5.50b}$$

Example 5.12 Determine the change in flat band voltage (threshold voltage) if 4 x 10^{11} Boron ions/cm^2 are implanted in the oxide at a depth of 0.07 μm from the surface. Let C_{ox} = 35 nF, t_{ox} =0.1 μm.

$$N_I = 4 \times 10^{11} \text{ cm}^{-2}$$

Implanted charge density $Q_I = qN_I$

$$= -1.6 \times 10^{-19} \times 4 \times 10^{11}$$

$$= -6.4 \times 10^{-8} \text{ C/cm}^2$$

$$\Delta V_{FB} = \Delta V_{th} = \frac{-Q_{I\,x}}{C_{ox} t_{ox}} \quad \text{(By equation 5.47a)}$$

$$= \frac{-6.4 \times 10^{-8} \times 0.07}{35 \times 10^{-9} \times 0.1}$$

$$= -1.28 \text{ V.}$$

5.4.6 Small Signal Equivalent Circuit

The low-frequency small signal equivalent circuit of a MOSFET is shown in Fig. 5.44.

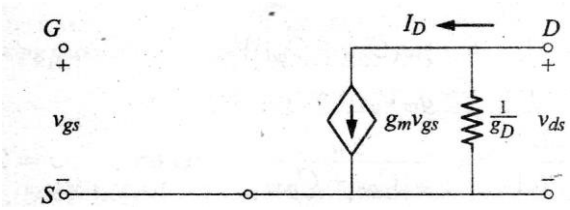


Fig. 5.44 Low-frequency small signal equivalent circuit of MOSFET

Transconductance $g_m = \left.\frac{\partial I_D}{\partial V_{GS}}\right|_{V_{DS\,(constant)}} \cong \sqrt{2k_p I_{D(sat)}}$

$= K_p(V_{GS} - V_{th})$ (by equation (5.45) (5.51)

Drain conductance $g_D = \left.\frac{\partial I_D}{\partial V_{DS}}\right|_{V_{GDS\,(constant)}} \cong \lambda_p I_{D(sat)}$ (5.52)

The small signal high-frequency equivalent circuit of a MOSFET is shown in Fig. 5.45.

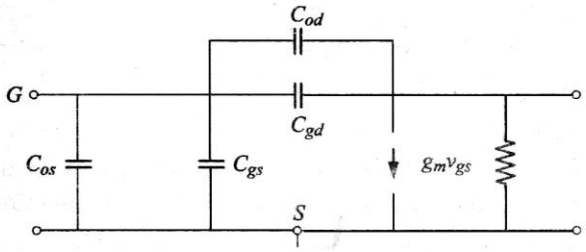


Fig. 5.45 High-frequency small signal equivalent circuit of a MOSFET

C_{od} - overlap capacitance between gate and drain
C_{os} - overlap capacitance between gate and source
C_{gs} - gate to source capacitance
C_{gd} - gate to drain capacitance.

5.4.7 Figure of Merit(f_T)

Figure of merit of a MOSFET is equal to the short-circuit unity gain bandwidth. To determine figure of merit of MOSFET consider the approximate equivalent circuit shown in Fig. 5.46.

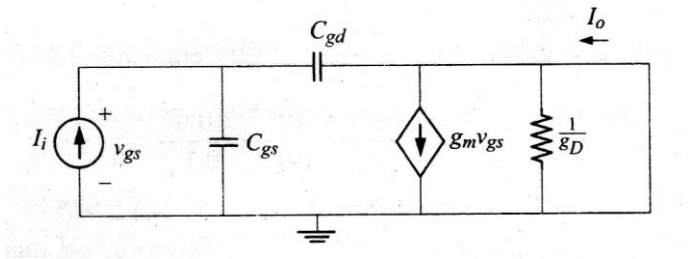


Fig. 5.46 Circuit to determine figure of merit of MOSFET. C_{gs} and C_{gd} comes in parallel as a result of short-circuit at the output.

$$I_i = j\omega\left(C_{gs} + C_{gd}\right)V_{gs}$$

$$I_o = g_m V_{gs}$$

$$\left|\frac{I_o}{I_i}\right| = \frac{g_m}{\omega\left(C_{gs} + C_{gd}\right)} \quad where \quad \omega = 2\pi f$$

$$f = f_T \quad when \quad \left|\frac{I_o}{I_i}\right| = 1$$

$$f_T = \frac{g_m}{2\pi\left(C_{gs} + C_{gd}\right)} \tag{5.53}$$

$[C_{gs} + C_{gd})$ may be replaced with $(C_{ox}ZL)$, which is the effective capacitance between gate and channel.

Substituting for g_m from equation (5.50)

$$f_T = \frac{k_p(V_{GS} - V_{th})}{2\pi ZLC_{ox}}$$

$$= \frac{\mu_p(V_{GS} - V_{th})}{2\pi L^2} \quad \left(\text{Q } k_p = \bar{\mu}_n \frac{C_{ox}Z}{L}\right) \tag{5.54}$$

MOSFET vs. BJT

The cost of fabrication of MOSFET is less than that of BJT. It is self isolating. Isolation is achieved by heavy dopings and thick oxides in the region between adjacent devices. MOS transistors take less space in ICs and require only less number of steps compared to BJT. BJTs require tubs for isolation between devices.

In digital circuits, MOS transistors do not conduct below the threshold voltage whereas conduction in BJT is a gradual process. MOS transistors consume less dc power. Under normal operating conditions transconductance is better for BJT. The cut-off frequency is higher for MOSFET (n channel) than that of npn BJT with base width equal to channel length and both made of silicon.

Solved Problems

Problem 5.1

It is required to use a JFET of Fig. Sp.5.1 as a linear resistor. The parameters of the JFET are as follows: Z = 100 μm, L = 10 μm, a = 2.5 μm. The doping in the n-layer (N_D) is $10^{16}/cm^3$ and the electron mobility is 1500 cm^2/Vs. The depletion layer width of each junction due to built-in potential is 0.25 μm. The two p^+ gate regions are connected together externally The resistance of the region outside the gate are negligible. Determine the minimum value of the linear resistor which can be realized using this JFET without forward-biasing the gate junctions.

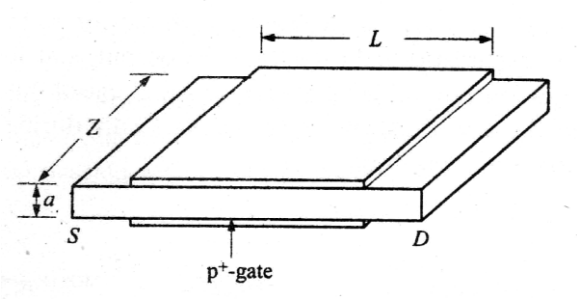


Fig. Sp. 5.1

Solution

$L = 10\ \mu m$

$\mu_n = 1500\ cm^2/Vs$

Depletion layer width at equilibrium (W_o) = 0.25 μm

Channel thickness $= a - 2W_o$

$= 2.5 - 2 \times 0.25 = 2.0\ \mu m$

The linear resistor has minimum value under equilibrium ($V_{GS} = 0$).

$$R_{(min)} = \rho_o \frac{L}{A} = \frac{1 \times L}{\sigma_o A}$$

$$= \frac{L}{qN_D\mu_n Z(a - 2W_o)}$$

$$= \frac{10 \times 10^{-4}}{1.6 \times 10^{-19} \times 10^{16} \times 1500 \times 100 \times 10^{-4} \times 2 \times 10^{-4}}$$

$= 208.33\ \Omega.$

Problem 5.2

An n-channel Si JFET has $N_A = 10^{19}\ cm^{-3}$ $N_D = 10^{15}\ cm^{-3}$ and a = 4 μm. Determine at 300 K (a) pinch-off voltage (b) the gate bias required to make the thickness of undepleted channel equal to 1μm with $V_{DS} = 0$.

Solution

a. $V_P = \frac{qN_D a^2}{2\grave{o}}$

$$= \frac{1.6 \times 10^{-19} \times 10^{15} \times \left(4 \times 10^{-4}\right)^2}{2 \times 8.854 \times 10^{-14} \times 11.8}$$

b. $2W$ = 2a - undepleted channel thickness

$= 2 \times 4 - 1 = 7\ \mu m$

$\therefore W = 3.5\ \mu m$

$W = \sqrt{\frac{2\grave{o}(V_o - V_{GS})}{qN_D}}$

$$V_0 - V_{GS} = \frac{qN_D W^2}{2\varepsilon}$$

$$= \frac{1.6\times10^{-19}\times10^{15}\times(3.5\times10^{-4})^2}{2\times8.854\times10^{-14}\times11.8} = 9.38 \text{ V}$$

$$V_0 = \frac{kT}{q} In \frac{N_A N_D}{n_i^2}$$

$$= 0.026 \text{ In}\left[\frac{10^{19}\times10^{15}}{(1.5\times10^{10})^2}\right] = 0.817 \text{ V}$$

$$V_{GS} = V_0 - 9.38 = 0.859 - 9.38$$

$$= -8.563 \text{ V}.$$

Problem 5.3

An n-channel Si JFET has $N_D = 10^{15}$ cm^{-3}, $N_A = 10^{18}$ cm^{-3} and a = 2.0 μm. Determine (a) built-in voltage, (b) pinch-off voltage, (c) threshold voltage.

Solution

a. Built-in voltage $V_0 = \frac{kT}{q} In \frac{N_A N_D}{n_i^2}$

$$= 0.026 \text{ In}\left[\frac{10^{18}\times10^{15}}{(1.5\times10^{10})^2}\right] = 0.757 \text{ V}$$

b. Pinch-off voltage $V_p = \frac{qN_D a^2}{2\grave{o}}$

$$= \frac{1.6\times10^{-19}\times10^{15}\times(2\times10^{-4})^2}{2\times 8.854\times10^{-14}\times11.8}$$

$$= 3.064 \text{ V}$$

c. Threshold voltage $V_{th} = V_0 - V_p$

$$= -2.307 \text{ V}.$$

Problem 5.4

An n-channel silicon JFET has $N_D = 5 \times 10^{16}$ cm^{-3}, $N_A = 10^{18}$ cm^{-3}, a = 0.5 μm. Determine at 300 K a. V_o b. $V_{(Dsat)}$ for V_{GS} = -3 V c. V_{GS} for $V_{D(sat)}$ = 1 V d. width of undepleted channel if V_{GS} = -2 V, V_{DS} = 0.

Solution

a. $V_0 = \frac{kT}{q} In \frac{N_A N_D}{n_i^2}$

$$= 0.026 \ln\left[\frac{10^{18} \times 5\times10^{16}}{\left(1.5 \times 10^{10}\right)^2}\right] = 0.858 \text{ V}$$

b. $V_{D(sat)} = V_P + V_{GS} - V_0$.

$$V_P = \frac{qN_D a^2}{2\grave{o}}$$

$$= \frac{1.6 \times10^{-19} \times5\times10^{16} \times(0.5\times10^{-4})^2}{2\times 8.854 \times10^{-14} \times11.8}$$

$$= 9.571$$

$$V_{D(sat)} = 9.571 + (-3) - 0.858$$

$$= 5.713 \text{ V}$$

c. $V_{GS} = V_{D(sat)} - V_P + V_0$.

$$= 1 - 9.571 + 0.858 = -7.713 \text{ V}$$

d. $$W = \sqrt{\frac{2\grave{o}(V_0 - V_{GS})}{qN_D}}$$

$$= \sqrt{\frac{2 \times 8.854\times 10^{-14} \times 11.8 \times (0.858 + 2)}{1.6 \times 10^{-19} \times 5 \times 10^{16}}}$$

$$= 0.273 \ \mu\text{m}$$

Width of undepleted channel $= 2a - 2W$

$$= 2 \times 0.5 - 2 \times 0.273$$

$$= 0.454 \ \mu\text{m}.$$

Problem 5.5

An n-channel silicon JFET has Z = 25μm , L = 5μm, a = 1.5 μm, $N_A = 10^{19}$ cm^{-3}. $N_D = 5 \times 10^{15}$ cm^{-3}, $\mu_n = 1200$ cm^2/Vs. At $V_{GS} = -3$ V. Determine:

a. drain current at saturation,

b. drain voltage at saturation and

c. transconductance at saturation.

Solution

a. By equation (5.7),

$$I_{D(sat)} = G_0\left[V_P - V_0 + V_{GS} - \frac{2V_P}{3} + \frac{2V_P}{3}\left(\frac{V_0 - V_{GS}}{V_P}\right)^{3/2}\right]$$

$V_{GS} = -3V$

$$G_0 = \frac{2q\mu_n N_D Za}{L}$$

$$= \frac{2 \times 1.6 \text{ x}10^{-19} \times 1200 \times 5 \times 10^{15} \times 25 \times 10^{-4} \times 1.5 \times 10^{-4}}{5 \times 10^{-4}}$$

$$= 1.44 \times 10^{-3} \text{ S} = 1.44 \text{ mS}$$

$$V_o = \frac{kT}{q} In \frac{N_A N_D}{n_i^2}$$

$$= 0.026 \text{ In}\left[\frac{10^{19} \times 5\times 10^{15}}{\left(1.5 \times 10^{10}\right)^2}\right] = 0.859 \text{ V}$$

$$V_p = \frac{qN_D a^2}{2\varepsilon}$$

$$= \frac{1.6 \times 10^{-19} \times 5\times 10^{15} \times (0.5\times 10^{-4})^2}{2\times 8.854 \times 10^{-14} \times 11.8}$$

$$= 8.61 \text{ V}$$

$$I_{D(sat)} = 1.44\times 10^{-3}\left[8.61 - 0.859 - 3 - \frac{2\times 8.61}{3} + \frac{2\times 8.61}{3}\left(\frac{0.859+3}{8.61}\right)^{3/2}\right]$$

$$= 1.06 \text{ mA}$$

b. $V_{D(sat)} = V_p + V_{GS} - V_0$

$$= 8.61\text{-}3\text{-}0.859$$

$$= 7.751 \text{ V}$$

c. Transconductance

$$g_m = G_0\left[1 - \left(\frac{V_0 - V_{GS}}{V_p}\right)^{1/2}\right]$$

$$= 1.44\times 10^{-3}\left[1 - \left(\frac{0.859+3}{8.61}\right)^{1/2}\right]$$

$$= 7.76 \times 10^{-4} \text{ A/V} = 0.476 \text{ mS}.$$

Problem 5.6

The avalanche break down voltage of the drain substrate junction of an n-channel JFET is 40 V. What will be the drain to source voltage at which avalanche breakdown occurs if V_{GS} = -3 V is applied.

Solution

Breakdown voltage at V_{GS} = 0 V, V_{Bro} = 40 V

Breakdown voltage at V_{GS} = -3 V = $V_{Bro} + V_{GS}$

= 40 + (-3) = 37 V.

Problem 5.7

An n-channel Si JFET has $N_A = 10^{19}$ cm^{-3}, No = 5×10^{15} cm^{-3}, L = 30 μm, Z = 200 μm; a = 1.5 μm. Assume μ_n = 1350 cm^2/Vs. Determine

a. the built-in voltage,

b. the pinch-off voltage,

c. the channel conductance G_o,

d. drain current at V_{GS} = 0; V_{DS} = 4 V,

e. $V_{D(sat)}$ for V_{GS} = 0 V, V_{GS} = -2 V, V_{GS} = -4 V,

f. $I_{D(sat)}$ for V_{GS} = -2 V and

g. g_m at V_{GS} = -2 V.

Solution

a. Built-in voltage

$$V_o = \frac{kT}{q} ln \frac{N_A N_D}{n_i^2}$$

$$= 0.026 \ln \left[\frac{10^{19} \times 5 \times 10^{15}}{\left(1.5 \times 10^{10}\right)^2} \right]$$

$$= 0.859 \text{ V}$$

$$V_p = \frac{qN_D a^2}{2\grave{o}}$$

$$= \frac{1.6 \times 10^{-19} \times 5 \times 10^{15} \times (0.5 \times 10^{-4})^2}{2 \times 8.854 \times 10^{-14} \times 11.8}$$

$$= 8.61 \text{ V}$$

(c) $$G_0 = \frac{2qN_D \mu_n Z_a}{L}$$

$$= \frac{2 \times 1.6 \times 10^{-19} \times 5 \times 10^{15} \times 1350 \times 200 \times 10^{-4} \times 1.5 \times 10^{-4}}{30 \times 10^{-4}}$$

$$= 2.16 \times 10^{-3}$$

(d) $V_{GS} = 0$, $V_{DS} = 4V$

$V_{D(sat)} = V_p + V_{GS} - V_0$

$= 8.61 + 0 - 0.859 = 7.751$ V

$V_{DS} < V_{D(sat)}$ ($\therefore$ By equation (5.6))

$$I_D = (f) \quad I_{D(sat)} = G_0 \left[V_{DS} - \frac{2}{3} V_P \left\{ \left(\frac{V_0 + V_{DS} - V_{GS}}{V_P} \right)^{3/2} - \left(\frac{V_0 - V_{GS}}{V_P} \right)^{3/2} \right\} \right]$$

$$= 2.16 \times 10^{-3} \left[4 - \frac{2}{3} \times 8.61 \left(\frac{0.859 + 4 - 0}{8.61} \right)^{1/2} - \left(\frac{0.859 - 0}{8.61} \right)^{3/2} \right]$$

$$= 3.77 \text{ mA}$$

(e) $V_{D(sat)} = V_P + V_{GS} - V_0$

when $V_{GS} = 0$, $V_{D(sat)} = 8.61 - 0.859 = 7.751$ V

$V_{GS} = -2$V, $V_{D(sat)} = 8.61 - 2 - 0.859 = 5.751$ V

$V_{GS} = -4$V, $V_{D(sat)} = 8.61 - 4 - 0.859 = 3.751$ V

$$I_{D(sat)} = G_0 \left[V_p - V_0 + V_{GS} - \frac{2}{3} V_p + \frac{2}{3} V_p \left(\frac{V_0 - V_{GS}}{V_p} \right)^{3/2} \right]$$

$$= 2.16 \times 10^{-3} \left[8.61 - 0.859 - 2 - \frac{2}{3} \times 8.61 + \frac{2}{3} \times 8.61 \left(\frac{0.859 + 2}{8.61} \right)^{3/2} \right]$$

$$= 2.39 \text{ mA}$$

g. By equation (5.11) $g_m = G_0 \left[1 - \left(\frac{V_0 - V_{GS}}{V_p} \right)^{1/2} \right]$

$$= 2.16\times10^{-3}\left[1-\left(\frac{0.859+2}{8.61}\right)^{1/2}\right]$$

$$= 9.158 \text{ x } 10^{-4} \text{ A/V} = 0.9158 \text{ mS.}$$

Problem 5.8

A uniformly doped single gate p-channel Si JFET has the following parameters at 300 K. $N_A = 5 \times 10^{15}$ cm^{-3}, $N_D = 5 \times 10^{19}$ cm^{-3}, L = 4 μm, Z = 50 μm, a = 1 μm. The hole mobility in the channel is 350 cm^2/Vs. For this JFET, calculate (a) pinch-off voltage V_p, (b) the gain band width product in the saturation region with $V_{GS} = 2$ V, (c) Repeat (a) and (b) if JFET is n-channel with same dimensions and dopings. Let $\mu_n = 1000$ cm^2/Vs and V_{GS} == -2 V.

Solution

a. Pinch-off voltage

$$V_p = \frac{qN_A a^2}{2\grave{o}}$$

$$= \frac{1.6\times10^{-19}\times5\times10^{15}\times(1\times10^{-4})^2}{2\times 8.854\times10^{-14}\times11.8}$$

$$= -3.829 \text{ V}$$

b. $$V_0 = \frac{kT}{q} ln \frac{N_A N_D}{n_i^2}$$

$$= 0.026 \ln\left[\frac{5\times10^{19}\times5\times10^{19}}{\left(1.5\times10^{10}\right)^2}\right] = 0.901 \text{ V}$$

$$G_o = qN_A\mu_p Za/L$$

$$= \frac{1.6\times10^{-19}\times 5\times10^{15}\times350\times50\times10^{-4}\times1\times10^{-4}}{4\times10^{-4}}$$

$$= 3.5\times10^{-4} \text{ A/V} = 0.35 \text{ mS}$$

In the saturation region

$$g_m = G_0\left[1-\left(\frac{-(V_0-V_{GS})}{V_P}\right)^{1/2}\right]$$

$$V_{GS} = +2V$$

$$\therefore g_m = 3.5\times10^{-4}\left[1-\left(\frac{0.901+2}{3.829}\right)^{\frac{1}{2}}\right]$$

$$= 4.55\times10^{-5} \text{ S}$$

$$C_{GS} = \frac{2\grave{o}ZL}{a}$$

$$= \frac{2\times8.854\times10^{-14}\times11.8\times50\times10^{-4}\times4\times10^{-4}}{1\times10^{-4}}$$

$$= 4.18\times10^{-14} \text{ F}$$

$f_T = \frac{g_m}{2\pi C_{GS}}$

$= \frac{4.55 \times 10^{-5}}{2 \times \pi \times 4.18 \times 10^{-14}} = 173.2 \times 10^8$ Hz

$= 173.2$ MHz

c. For n-channel JFET $N_D = 5 \times 10^{15}$ $N_A = 5 \times 10^{19}$

$V_p = \frac{qN_D a^2}{2\grave{o}}$

$= \frac{1.6 \times 10^{-19} \times 5 \times 10^{15} \times (1 \times 10^{-4})^2}{2 \times 8.854 \times 10^{-14} \times 11.8}$

$= 3.829$ V

b. $V_0 = \frac{kT}{q} In \frac{N_A N_D}{n_i^2}$

$= 0.026 \text{ In} \left[\frac{5 \times 10^{15} \times 5 \times 10^{19}}{(1.5 \times 10^{10})^2} \right] = 0.901$ V

$G_o = qN_D\mu_n Za / L$

$= \frac{1.6 \times 10^{-19} \times 5 \times 10^{15} \times 1000 \times 50 \times 10^{-4} \times 1 \times 10^{-4}}{4 \times 10^{-4}}$

$= 10^{-3}$ A/V = 1 mS

$g_m = G_0 \left[1 - \left(\frac{(V_0 - V_{GS})}{V_p} \right)^{1/2} \right]$

$= 10^{-3} \left[1 - \left(\frac{0.901 + 2}{3.829} \right)^{\frac{1}{2}} \right]$

$= 1.3 \times 10^{-4}$ S

= 13 mS

$C_{GS} = \frac{2\grave{o}ZL}{a}$

$= \frac{2 \times 8.854 \times 10^{-14} \times 11.8 \times 50 \times 10^{-4} \times 4 \times 10^{-4} \times 10^{-4}}{1 \times 10^{-4}}$

$= 4.18 \times 10^{-14}$

$f_T = \frac{g_m}{2\pi C_{GS}}$

$= \frac{1.3 \times 10^{-4}}{2\pi \times 4.18 \times 10^{-14}}$

$= 4.949 \times 10^8$ Hz = 494.9 MHz.

Problem 5.9

A gold n-channel GaAs MESFET has $N_D = 10^{16}$ cm^{-3}, a = 0.5 μm, L = 1 μm, z = 100 μm and μn = 7000 cm^2/Vs. Determine at room temperature.

a. the pinch-off voltage,

b. the threshold voltage,

c. find whether it is depletion or enhancement type

d. saturation drain current at $V_{GS} = 0$.

$\phi_B = 0.9$ V, n_i, $= 1.7 \times 10^6$ cm^{-3}

Solution

a. $V_P = \dfrac{qN_D a^2}{2\grave{o}}$

$= \dfrac{1.6\times10^{-19}\times10^{16}\times\left(0.5\times10^{-4}\right)^2}{2\times8.854\times10^{-14}\times13.1} = 1.72$ V

b. $V_{th} = V_o - V_P$

$V_o = \phi_B - \dfrac{E_g}{2} + \phi_F$

$\phi_F = \dfrac{kT}{q}\ln\dfrac{N_D}{n_i} = 0.026 \ln\left(\dfrac{10^{16}}{1.7\times10^6}\right)$

$= 0.585$ V

$V_o = 0.9 - \dfrac{1.43}{2} + 0.585 = 0.77$ V

$V_{th} = 0.77 - 1.72$

$= -0.95$ V

c. $V_{th} < 0$. The device is normally ON. Therefore this is a depletion type MESFET.

d. Saturation drain current with $V_{GS} = 0$

$I_{D(sat)} = G_0\left[V_P - V_0 - \dfrac{2}{3}V_P + \dfrac{2}{3}V_P\left(\dfrac{V_0}{V_P}\right)^{3/2}\right]$

$G_0 = \dfrac{qN_D\mu_n Za}{L}$

$= \dfrac{1.6\times10^{-19}\times10^{16}\times7000\times100\times10^{-4}\times0.5\times10^{-4}}{1\times10^{-4}}$

$= 0.056 = 56$ mS

$I_{D(sat)} = 0.056\left[1.72 - 0.77 - \dfrac{2}{3}\times1.72 + \dfrac{2}{3}\times1.72\left(\dfrac{0.77}{1.72}\right)^{3/2}\right]$

$= 8.22$mA.

Problem 5.10

Show that for an enhancement MESFET, the saturated drain current can be expressed as

$I_{D(sat)} = \dfrac{Z\mu_n\grave{o}}{2aL}(V_{GS} - V_{th})^2$

Solution

For a normally OFF MESFET,

$$V_P = \frac{qN_D a^2}{2\grave{o}} < V_o; \quad V_{th} = V_o - V_P$$

or $$V_o = V_{th} + V_P \qquad (A)$$

$$V_P = V_{D(sat)} + V_o - V_{GS}$$

$$V_{D(sat)} = V_P - V_o + V_{GS} = V_{GS} - V_{th} \qquad (B)$$

Substituting equations (A) and (B) in equation (5.7)

$$I_{D(sat)} = G_0\left[(V_{GS} - V_{th}) - \frac{2}{3}V_P\left\{1 - \left(\frac{V_{th} + V_P - V_{GS}}{V_P}\right)^{3/2}\right\}\right]$$

$$= G_0\left[(V_{GS} - V_{th}) - \frac{2}{3}V_P\left\{1 - \left(1 - \frac{(V_{GS} - V_{th})}{V_P}\right)^{3/2}\right\}\right]$$

As $\frac{V_{GS}-V_{th}}{V_P} << 1$

$$I_{D(sat)} = G_0\left[(V_{GS} - V_{th}) - \frac{2}{3}V_P\left\{\frac{2}{3}\left(\frac{V_{GS} - V_{th}}{V_P}\right)^2\right\}\right]$$

$$= \frac{G_o}{4V_P}(V_{GS} - V_{th})^2 = \frac{Z\mu_n\grave{o}}{2aL}(V_{GS} - V_{th})^2$$

$$\left(\text{Q} \quad G_o = \frac{qN_D\mu_n Za}{L} \text{ and } V_P = \frac{qN_D a^2}{2\grave{o}}\right)$$

Problem 5.11

A GaAs MESFET uses gold as a Schottky barrier gate. The channel doping is $N_D = 10^{16}$ cm^{-3}. Channel width = 0.6 μm. At 300 K, determine:

a. the pinch-off voltage,

b. the built-in voltage,

c. the threshold voltage and

d. determine the channel width so that the device is OFF when $V_{GS} = 0$.

($\phi_B = 0.88$ V, $n_i = 1.79 \times 10^6$ cm^{-3}

Solution

a. $$V_P = \frac{qN_D a^2}{2\grave{o}}$$

$$= \frac{1.6\times10^{-19}\times10^{16}(0.6\times10^{-4})^2}{2\times8.854\times10^{-14}\times13.1}$$

$$= 2.483 \text{ V}$$

b. $V_o = \phi_B - \frac{E_C - E_F}{q}$

$E_C - E_F = \frac{E_g}{2} - (E_F - E_i)$

$E_F - E_i = \frac{kT}{q} \ln \frac{N_D}{n_i}$

$= 0.026 \ln \left(\frac{10^{16}}{1.79 \times 10^6} \right) = 0.585$ V

$E_C - E_F = \frac{1.43}{2} - 0.584 = 0.131$ eV

$V_o = 0.88 - 0.131 = 0.749$ V

$V_{th} = V_o - V_P$

$= 0.749 - 2.483 = -1.734$ V

d. $W_o = \sqrt{\frac{2\grave{o}V_0}{qN_D}}$

$= \sqrt{\frac{2 \times 13.1 \times 8.854 \times 10^{-14} \times 0.749}{1.6 \times 10^{-19} \times 10^{16}}}$

$= 0.32$ μm.

If the channel width is less than or equal to 0.32 μm, the device will be off when $V_{GS} = 0$.

Problem 5.12

A MOS capacitor with silicon substrate of doping $N_A = 5 \times 10_{16}$ cm^{-3} has oxide thickness of 100 Å. Calculate the applied voltage, the electric field intensity at the interface and the depletion layer width (a) to make semiconductor surface intrinsic (b) for strong inversion.

Solution

a. When the semiconductor surface is intrinsic

$\phi_s = \phi_F = \frac{kT}{q} \ln \frac{N_A}{n_i}$

$= 0.026 \ln \left(\frac{5 \times 10^{16}}{1.5 \times 10^{10}} \right)$

$= 0.391$ V

$W = \sqrt{\frac{2\grave{o}\phi_F}{qN_A}}$

$= \sqrt{\frac{2 \times 8.854 \times 10^{-14} \times 11.8 \times 0.391}{1.6 \times 10^{-19} \times 5 \times 10^{16}}}$

$= 1.01 \times 10^{-5}$ cm

$Q_s = -qN_AW$

$= -1.6 \times 10^{-19} \times 5 \times 10^{16} \times 1.01 \times 10^{-5}$

$= -8.08 \times 10^{-8}$ C/cm^2

$C_{ox} = \frac{\grave{o}_{ox}}{t_{ox}}$

$$= \frac{8.854\times10^{-14}\times3.9}{100\times10^{-8}} = 3\text{-}453 \times 10^{-7}$$

$$V_G = \frac{-Q_S}{C_{ox}} + \phi_S$$

$$= \frac{8.08\times10^{-8}}{3.453\times10^{-7}} + 0.391$$

Electric field intensity at interface

$$E_m = \frac{q}{\grave{o}_{sc}} N_A W$$

$$= \frac{1.6\times10^{-19}\times5\times10^{16}\times1.01\times10^{-5}}{8.854\times10^{-14}\times11.8}$$

$$= 77337.45 \text{ V/cm}$$

b. At strong inversion

$$\phi_s = 2\phi_F = 2 \times 0.391 = 0.782 \text{ V}$$

$$W_m = \sqrt{\frac{4\grave{o}\phi_F}{qN_A}}$$

$$= \sqrt{\frac{4\times8.854\times10^{-14}\times11.8\times0.391}{1.6\times10^{-19}\times5\times10^{16}}}$$

$$= 1.429 \times 10^{-5} \text{ cm}$$

$$Q_{Dm} = -qN_A W_m$$

$$= -1.6 \times 10^{-19} \times 5 \times 10^{16} \times 1.429 \times 10^{-5}$$

$$= -1.413 \times 10^{-7} \text{ C/cm}^2$$

$$E_m = \frac{q}{\grave{o}_{sc}} N_A W_m$$

$$= \frac{1.6\times10^{-19}\times5\times10^{16}\times1.429\times10^{-5}}{8.854\times10^{-14}\times11.8}$$

$$= 1.094 \times 10^5 \text{ V/cm}$$

Problem 5.13

A silicon MOS system with p-type substrate with $N_A = 10^{15}$ cm^{-3} and oxide thickness 100 Å is at the onset of strong inversion. Determine:

a. width of depletion layer,

b. the charge density in the depletion layer,

c. the electron density n, at the surface and

d. the threshold voltage.

$\in r_{ox} = 3.9$

Solution

a. $$W_m = \sqrt{\frac{2\grave{o}2\phi_F}{qN_A}}$$

$$\phi_F = \frac{kT}{q} \ln \frac{N_A}{n_i}$$

$$= 0.026 \ln \frac{10^{15}}{1.5\times10^{10}} = 0.2887 \text{ V}$$

$$W_m = \sqrt{\frac{2\times8.854\times10^{-14}\times11.8\times2\times0.2887}{1.6\times10^{-19}\times10^{15}}}$$

$$= 8.684 \times 10^{-5} \text{ cm}$$

b. $Q_{Dm} = -qN_AW_m$

$$= -1.6 \times 10^{-19} \times 10^{15} \times 8.684 \times 10^{-5}$$

$$= 13.894 \times 10^{-19} \text{ C/cm}^2$$

c. $n_s = n_{po}\ e^{2\phi_F/V_T}$

$$n_{po} = \frac{n_i^2}{N_A} = \frac{\left(1.5\times10^{10}\right)^2}{10^{15}}$$

$$= 2.25 \times 10^5 \text{ cm}^{-3}$$

$$= 2.25 \times 10^5\ e^{\frac{2\times0.2887}{0.26}}$$

$$= 9.927 \times 10^{14} \text{ cm}^{-3}.$$

d. $V_{th} = 2\phi_F - \frac{Q_{Dm}}{C_{ox}}$

$$C_{ox} = \frac{\in_{ox}}{t_{ox}} = \frac{8.854\times10^{-14}\times3.9}{100\times10^{-8}}$$

$$= 3.45 \times 10^{-7} \text{ F/cm}^2$$

$$V_{th} = 2 \times 0.2887 - \frac{13.894\times10^{-9}}{3.45\times10^{-7}}$$

$$= 0.537\text{V}.$$

Problem 5.14

Determine the flat band voltage and threshold voltage of a p-MOS device that has silicon 'n' substrate with $N_D = 10^{15}$ cm^{-3} which use Al as gate. $Q_{ox} = 5 \times 10^{10}$ qC/cm^2.
$\in_{rox} = 3.9$, $t_{ox} = 200$ Å, $\in_{rsi} = 11.8$, $E_g = 1.12$ eV, $\psi_{sc} = 4.15$ V, $\phi_m = 4.2$ V.

Solution

$$\phi_F = -\frac{kT}{q}\ln\frac{N_A}{n_i}$$

$$= -0.026 \ln\left(\frac{10^{15}}{1.5\times10^{10}}\right) = 0.289 \text{ V}$$

$$\phi_{ms} = (\phi_m - \phi_{sc})$$

$$= \left[\phi_m - \left(\psi_{sc} + \frac{E_g}{2q} + \phi_F\right)\right]$$

$$= \left[4.2 - \left(4.15 + \frac{1.12}{2} - 0.289\right)\right]$$

$$= -0.221 \text{ V}$$

$$C_{ox} = \frac{\grave{o}_{ox}}{t_{ox}}$$

$$= \frac{8.854\times10^{-14}\times3.9}{200\times10^{-8}} 1.726 \times 10^{-7} \text{ F/cm}^2$$

$$\frac{Q_{ox}}{C_{ox}} = \frac{5\times10^{-10}\times1.6\times10^{-19}}{1.726\times10^{-7}} = 0.046 \text{ V}$$

$$Q_{Dm} = qN_D W_m$$

$$W_m = \sqrt{\frac{4\grave{o}\phi_F}{qN_D}}$$

$$= \sqrt{\frac{4\times8.854\times10^{-14}\times11.8\times0.289}{1.6\times10^{-19}\times10^{15}}}$$

$$= 8.688 \times 10^{-5} \text{ cm}$$

$$Q_{Dm} = 1.6 \times 10^{-19} \times 10^{15} \times 8.688 \times 10^{-5}$$

$$= 13.9 \times 10^{-9} \text{ C/cm}^2$$

$$V_{FB} = \phi_{ms} - \frac{Q_{ox}}{C_{ox}} = -0.221 - 0.046 = -0.267 \text{ V}$$

$$V_{th} = \phi_{ms} - \frac{Q_{ox}}{C_{ox}} - \frac{Q_{Dm}}{C_{ox}} + 2\phi_F$$

$$= -0.221 - 0.046 - \frac{13.9\times10^{-9}}{1.726\times10^{-7}} + 2 \times -0.289$$

$$= -0.9255 \text{ V}.$$

Problem 5.15

Explain the procedure for the measurement of transconductance parameter (k_p) and threshold voltage of a MOSFET.

Solution

The experimental set up for the measurement of MOSFET parameters (k_p and V_{th}) are shown in Fig. Sp.5.15.

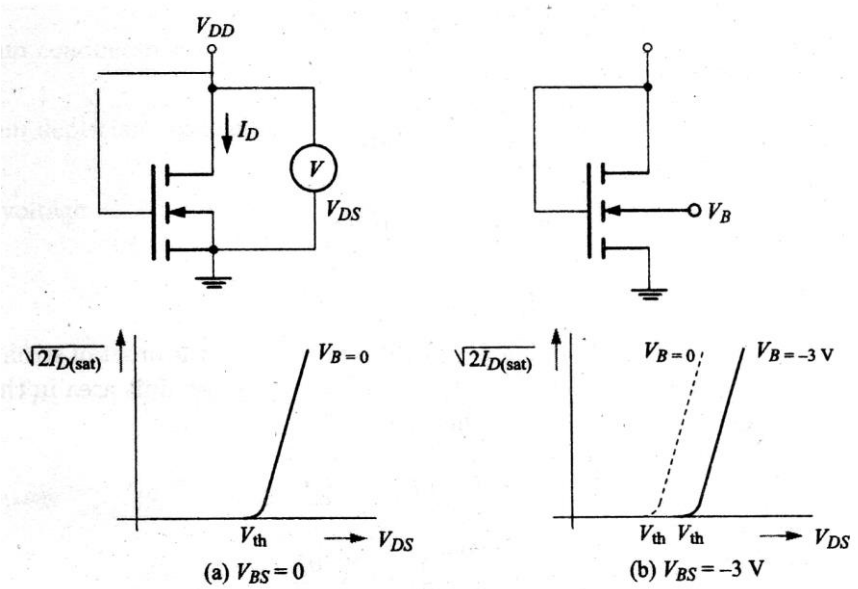


Fig. Sp.5.15 Measurement of V_{th} and k_p of MOSFET

$$I_{D(sat)} = \frac{k_p}{2}(V_{GS} - V_{th})^2; \quad V_{GS} \geq V_{th} \text{ and } V_{DS} \geq V_{GS} - V_{th}$$

Make a plot of $\sqrt{2I_{D(sat)}}$ vs V_{DS} which will be linear.

$$\sqrt{k_p} = \frac{\sqrt{2I_{D(sat)}}}{V_{GS} - V_{th}}$$

which is the slope of the above plot. Therefore k_p may be calculated as the square of the slope.

The intercept on the voltage axis gives the value of V_{th} (when $I_{D(sat)} = 0$; $V_{GS} = V_{th}$). To study the effect of V_B on V_{th} apply a positive voltage to the substrate (V_g) and plot the characteristics again. The new intercept on X-axis gives modified value of V_{th} as shown in Fig. Sp.5.15(b).

Problem 5.16

A silicon n substrate is doped with $N_D = 5 \times 10^{15}$ cm^{-3}. Determine the surface potential needed to make the surface (a) intrinsic and (b) strong inversion.

Solution

$$\phi_F = \frac{-kT}{q} \ln \frac{N_D}{n_i}$$

$$= 0.026 \ln \frac{5 \times 10^{15}}{1.5 \times 10^{10}} = -0.33 \text{ V}$$

(a) For intrinsic surface:

$$\phi_s = \phi_F = -0.33\text{V}$$

(b) For strong inversion:

$$\phi_s = 2\phi_F$$
$$= 2 \times -0.33 \text{ V}$$
$$= -0.66 \text{ V}$$

Problem 5.17

For silicon with p substrate doping $N_A = 10^{15}$ cm^{-3} and at the onset of strong inversion, calculate: (a) the width of depletion layer (b) the charge per unit area in the depletion layer (c) the electron density n_s at the surface.

Solution

(a) $W_m = \sqrt{\frac{4\grave{o}\phi_F}{qN_A}}$

$\phi_F = \frac{kT}{q}\ln\frac{N_A}{n_i}$

Assume $n_i = 1.5 \times 10^{10}$ cm^{-3}

$\phi_F = 0.026 \ln \frac{10^{15}}{1.5\times10^{10}} = 0.288$ V

$W_m = \sqrt{\frac{4\times8.854\times10^{-14}\times11.8\times0.288}{1.6\times10^{-19}\times10^{15}}}$

$= 8.67 \times 10^{-5}$ cm $= 0.867$ μm

(b) $Q_{dm} = -qN_AW_m$

$= 1.6 \times 10^{-19} \times 10^{15} \times 8.67 \times 10^{-5}$

$= 13.9 \times 10^{-8}$ C/cm^2

(c) $n_s = n_{po}e^{2q\phi F/kT}$

$n_{po} = \frac{n_i^2}{N_A} = \frac{\left(5\times10^{10}\right)^2}{10^{15}}$

$= 2.25 \times 10^5$ cm^{-3}

$n_s = 2.25 \times 10^5 \; e^{\frac{2\times0.288}{0.0259}}$

$= 1.02 \times 10^{15}$ cm^{-3}

▪ Points to Remember

JFET

- Equilibrium conductance $G_0 = \frac{2q\mu_n N_D(a-W_0)}{L}$
- Equilibrium depletion layer width $W_0 = \sqrt{\frac{2\in V_0}{qN_D}}$
- Pinch-off voltage $V_P = \frac{qN_Da^2}{2\grave{o}}$

$V_P = V_{D(sat)} + V_0 - V_{GS}$

$$I_D = G_0\left[V_{DS} - \frac{2}{3}V_P\left\{\frac{V_0 + V_{DS} - V_{GS}}{V_P}\right\}^{3/2} - \left(\frac{V_0 - V_{GS}}{V_P}\right)^{3/2}\right]$$

$$I_{D(sat)} = G_0\left[V_P - V_0 + V_{GS} - \frac{2}{3}V_P + \frac{2}{3}V_P\left(\frac{V_0 - V_{GS}}{V_P}\right)^{3/2}\right]$$

Channel conductance

$$g_D = G_0\left[1 - \left(\frac{V_0 + V_{DS} - V_{GS}}{V_P}\right)^{1/2}\right]$$

In linear region $g_D = G_0\left[1 - \left(\frac{V_0 - V_{GS}}{V_P}\right)^{1/2}\right]$

Transconductance $g_m = G_0\left[\left(\frac{V_0 + V_{DS} - V_{GS}}{V_P}\right)^{1/2} - \left(\frac{V_0 - V_{GS}}{V_P}\right)^{1/2}\right]$

At pinch-off, $g_m = G_0\left[1 - \left(\frac{V_0 - V_{GS}}{V_P}\right)^{1/2}\right]$

- $I_{D(sat)} = I_{DSS}\left[1 + \left(\frac{V_{GS}}{V_P}\right)\right]^2$
- Figure of merit $f_T = \frac{g_m}{2\pi(C_{gs} + C_{gd})}$

  or $f_T = \frac{q\mu_n a^2 N_D}{4\pi\grave{o}L^2}$

- **MESFET**

  $V_P = \frac{qN_D a^2}{2\grave{o}}$

$V_{th} = V_0 - V_p$

Enhancement MESFET is normally OFF; $V_{th} > 0$.

Depletion MESFET is normally ON; $V_{th} < 0$.

- For ideal MOS capacitor

$$W = \sqrt{\frac{2\grave{o}\phi_s}{qN_A}}$$

$$W_m = \sqrt{\frac{4\grave{o}\phi_F}{qN_A}}$$

At the onset of inversion $\phi_S = \phi_F$

At strong inversion $\phi_S = 2\phi_F$

$$V_{th} = \frac{-QD_m}{C_{ox}} + 2\phi_F$$

Real MOS capacitor

$$V_{th} = V_{FB} - \frac{QD_m}{C_{ox}} + 2\phi_F$$

$$V_{FB} = \phi_{ms} - \frac{Q_{ox}}{C_{ox}}$$

MOSFET

$$V_{th} = V_{FB} - \frac{Q_{Dm}}{C_{ox}} + 2\phi_F$$

$$I_D = \bar{\mu}_n C_{ox} \frac{Z}{L}\left[(V_{GS} - V_{th})V_{GS} - \frac{V_{DS}^2}{2}\right]$$

$$I_{D(sat)} = \frac{k_p}{2}(V_{GS} - V_{th})^2$$

$$k_p = \bar{\mu}_n C_{ox} \frac{Z}{L}$$

- Change in threshold voltage with substrate bias, $\Delta V_{th} = \gamma\sqrt{2\phi_F - V_B} - \sqrt{2\phi_F}$ where $\gamma = \frac{\sqrt{2\grave{o}qN_A}}{C_{ox}}$ is the body factor.
- Change in threshold voltage by implantation of impurity in the substrate (at oxide semi conductor interface)

$$\Delta V_{th} = \frac{-Q_I}{C_{ox}}$$

where Q_I represent the implanted charge per unit area.

Figure of merit $f_T = \frac{g_m}{2\pi(C_{gs} + C_{gd})}$

$$= \frac{k_p(V_{GS} - V_{th})}{2\pi ZLC_{ox}}$$

▪ Exercise Problems

(1) An n-channel dual gate Si JFET at 300 K has $N_D = 5 \times 10^{15}$ cm^{-3}, $N_A = 10^{19}$ cm^{-3}, a=l μm, L = 5 μm, Z = 20 μm. Determine the built-in voltage and pinch-off voltage.
Ans: $V_o = 0.859$ V, $V_P = 3.83$ V.
(2) For the JFET described in problem (1), determine
(a) $I_{D(sat)}$ at $V_{GS} = 0$,
(b) the gate voltage at which $I_D = 0$ for all V_{DS} (cut-off voltage).
Assume $\mu_n = 1000$ cm^2/Vs.
Ans: (a) 4.409×10^{-5} A, (b) -2.971 V.
(3) Determine an expression for maximum value of gm of an n-channel JFET.
Ans: G_o.
(4) An n-channel Si JFET has $N_D = 5\times 10^{15}$ cm^{-3} and $N_A = 10^{19}$ cm^{-3} and a = 2.5 μm.

Determine the gate voltage at which the width of the undepleted channel equals 1 μm with $V_{DS} = 0$.

Ans: -14.44 V.

(5) An n-channel Si JFET has Z = 20 μm, L = 5 μm, a = 2 μm, $N_A = 10^{19}$ cm^{-3}, $N_D = 5 \times 10^{15}$ cm^{-3} and $\mu_n = 1000$ cm^2 / Vs. If $V_{GS} = -3$ V, determine

(a) $I_{D(sat)}$

(b) $V_{D(sat)}$.

Ans: (a) 3.247 mA, (b) 11.455 V.

(6) An n-channel JFET has $V_P = 5$ V, $V_o = 0.8$ V and $I_{DSS} = 10$ mA. Determine

(a) G_o,

(b) $I_{D(sat)}$ at $V_{GS} = -3$V and

(c) g_m at $V_{GS} = -3$ V in saturation region.

Ans: (a) 9.234 mS, (b) 1.6 mA, (c) 1.184 mS.

(7) A GaAs MESFET with gold as the gate metal and channel doping of 10^{16} cm^{-3} has a = 0.8 μm, L = 5 μm, Z = 20 μm, $\mu_n = 6000$ cm^2/Vs and $\epsilon_r = 13.1$. Determine the threshold voltage and the type of MESFET. $\phi_{Bm} = 0.9$ V.

Ans: $V_{th} = -3.612$ V, depletion type.

(8) A GaAs MESFET with gold as gate metal has $N_D = 10^{16}$ cm^{-3} and a = 1μm at 300 K. Determine

(a) the pinch-off voltage,

(b) the built-in voltage,

(c) the threshold voltage and

(d) type of MESFET (enhancement or depletion) given $\phi_{Bm} = 0.9$ V.

Ans: (a) 6.84 V, (b) (b) 0.769 V, (c) -6.07 V, (d) depletion.

(9) Determine the maximum channel thickness so that the above MESFET is OFF when $V_{GS} = 0$.

Ans: 3.6×10^{-5} cm.

(10) A GaAs MESFET operating at 300 K has the following parameters. $\phi_B = 0.8$ V, a =1 μm, L = 10 μm, Z = 20 μm, $N_D = 10^{16}$ cm^{-3}, $\mu_n = 6500$ cm^2/Vs.

Determine

(a) $I_{D(sat)}$ at $V_{GS} = 0$ and $V_{GS} = -1$ V

(b) g_m at saturation with $V_{GS} = 0$ and $V_{GS} = -1$ V.

Ans: (a) 2.417 mA, (b) 1.053 mS.

(11) A MOS capacitor with gold as gate metal is formed on n-type Si substrate with $N_D = 10^{15}$ cm^{-3}. The oxide thickness is 250 A and oxide charge density (Q_{ox}) is 5×10^{10} q C/cm^2, $\epsilon_{rox} = 3.9$, $\phi_m = 4.7$ V, $\psi_s = 4.2$ V. Determine

(a) the flat band voltage,

(b) threshold voltage.

Ans: (a) -0.397 V, (b) -1.075 V.

(12) A MOS capacitor formed on n-type silicon substrate is doped with $N_D = 5 \times 10^{16}$ cm^{-3}, determine the surface potential required to make the surface

(a) intrinsic,

(b) at strong inversion.

Ans: (a) -0.3905 V, (b) -0.781 V.

(13) Calculate the maximum width of depletion layer of a MOS capacitor made on a silicon substrate with $N_A = 5 \times 10^{16}$ cm^{-3}.

Ans: 1.428×10^{-5} cm.

(14) A silicon MOS capacitor is doped with $N_A = 10^{16}$ cm^{-3} and has an oxide thickness of 200 A. Calculate the gate voltage and depletion layer width for

(a) intrinsic semiconductor surface,

(b) strong inversion.

Ans: (a) 0.547 V, 2.135×10^{-5} cm, (b) 0.9778 V, 3.019×10^{-5} cm.

(15) Calculate the threshold voltage of an ideal ($\phi_{ms} = 0, Q_{ox} = 0$) n-channel MOSFET with t_{ox} = 100 Å and $N_A = 10^{15}$ cm^{-3}.

Ans: 0.618V.

(16) Calculate the capacitance per unit area of an ideal MOS capacitor with $N_A = 10^{15}$ cm^{-3} and t_{ox} = 100 Å under accumulation and strong inversion. Oxide used is SiO_2.

Plot the C-V diagram.

Ans: 3.453×10^{-7} F/cm^2, low frequency: 3.45×10^{-7} F/cm^2, high frequency: 1.161×10^{-8} F/cm^2.

(17) An NMOS silicon transistor has $N_A = 10^{15}$ cm^{-3}, t_{ox} = 100 A, L = 2 μm, Z = 10 μm, $\bar{\mu}_n$ = 800 cm^2/Vs and V_{FB} = -0.2 V. Using square law model determine the drain current at V_{GS} = +5 V and V_{DS} = 4 V.

Ans: 1.426 mA.

(18) An n-channel MOSFET has following parameters $\frac{Z}{L}$ = 5, V_{FB} = 0.25 V, $N_A = 10_{17}$ cm^{-3}, $\bar{\mu}_n$ = 750 cm^2/ Vs, t_{ox}= 100 A°. For V_{GS} = 5 V determine

(a) $I_{D(sat)}$.

(b) $V_{D(sat)}$.

Ans: (a) 7.724 mA, (b) 3.454 V.

(19) An n-channel MOSFET has following parameters $\frac{Z}{L}$ = -10, V_{th} = 0.6 V, $\bar{\mu}_n$ = 600 cm^2/Vs, t_{ox} = 200 A. At V_{GS} =4 V, determine

(a) I_D, g_m and g_D if V_{DS} = 7 V,

(b) I_D, g_m and g_D if V_{DS} = 2 V.

Ans: (a) 6.98 mA, 8.456×10^{-3} S, 4.107×10^{-3} S.

(b) 5.798 mA, 2.416×10^{-3} S, 4.107×10^{-3} S.

(20) A silicon n-channel MOS uses aluminium as gate and has $N_A = 5 \times 10^{15}$ cm^{-3} and t_{ox} = 100 A°, $\frac{Z}{L}$ = 10, $\bar{\mu}_n$ = 700 cm^2/Vs. It is used as a voltage variable resistor.

Determine the value of the resistor at

(a) V_{GS} = 5 V,

(b) V_{GS} = 10 V.

Ans: (a) 97.56 Ω, (b) 44.76 Ω

▪ Review Questions

(1) What are the advantages of FETs over BJT?
(2) What is meant by 'field effect' transistor?
(3) How are FETs classified?
(4) Why is n channel FET preferred over p channel FET?
(5) Explain the fabrication of JFET.

(6) Explain the principle of operation of JFET.
(7) Define (a) pinch-off voltage (b) saturation voltage and (c) threshold voltage of JFET.
(8) Derive ah expression for equilibrium conductance (Go) of n channel JFET.
(9) Write the expression for pinch-off voltage in terms of (a) channel doping and channel thickness (b) saturation voltage and gate to source voltage.
(10) Draw the cross-sectional view of the channel along with depletion layers under pinch-off condition.
(11) Draw the drain characteristics of a JFET and explain.
(12) Derive expression for drain current of JFET. What are the approximations used?
(13) How is the expression in question 12 modified under saturation condition?
(14) Derive expressions for transconductance and drain resistance of JFET in linear and saturation regions.
(15) What is meant by channel length modulation in JFET?
(16) What is the effect of increase in temperature on JFET drain current?
(17) Draw the high frequency small signal model of JFET and derive expression for figure of merit.
(18) What are the advantages of MESFET over JFET?
(19) What is the difference between enhancement and depletion MESFET's?
(20) Write expressions for pinch-off voltage and threshold voltage of MESFET.
(21) Why are MESFET's usually of n channel type?|
(22) How do expression for drain current of MESFET differ from that of JFET?
(23) Draw the transfer and drain characteristics of enhancement and depletion type MESFETs.
(24) What are the mobility models used for MESFETs?
(25) Draw a simplified structure of MOS capacitor.
(26) Draw the energy band diagram of MOS capacitor under
(a) thermal equilibrium
(b) accumulation
(c) depletion
(d) inversion
(e) strong inversion.
(27) What is the value of surface potential of a MOS capacitor under (a) at the onset of inversion (b) strong inversion?
(28) Draw a set-up to measure CV characteristics of a MESFET and explain.
(29) Draw the C-V characteristics of an ideal MOS capacitor and explain.
(30) Define threshold voltage of ideal MOS capacitor.
(31) What is meant by flat band voltage?
(32) What are the non-idealities in a real MOS capacitor? How do they change flat band voltage and threshold voltage?
(33) What are the different types of charges present in the oxide? How do they affect the threshold voltage of MOS system?
(34) Explain variation of threshold voltage with substrate doping for a MOS capacitor with p-type and n-type substrates.
(35) What is the difference between MOSFET and MESFET?

(36) What is the difference between enhancement and depletion MOSFETs? Draw the transfer and drain characteristics.
(37) Explain the fabrication of MOSFET.
(38) Draw the cross-section of a MOSFET showing channel and depletion regions under (a) strong inversion (b) pinch-off (c) cut-off.
(39) Derive expression for drain current of MOSFET (use square law model). What are the approximations used?
(40) What is meant by threshold voltage of a MOSFET?
(41) What is meant by body effect?
(42) What are the non-idealities in a real MOSFET?
(43) What is meant by channel length modulation in MOSFET?
(44) What are the precautions required while handling MOSFETs? Why?
(45) What is meant by ESD in MOSFETs?
(46) What are the factors affecting threshold voltage of a MOSFET?
(47) What is meant by threshold tailoring implant?
(48) What is channel stop implantation in MOSFETs?
(49) Draw the small signal equivalent circuit of MOSFET.
(50) Derive the expression for figure of merit of a MOSFET.