PART - II

Introduction to Fabrication Technology

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Introduction To Fabrication Technology

INTRODUCTION

Nowadays most of the electronic devices are fabricated using integrated circuit technology. With the advancement in fabrication technology, the dimensions of the devices go on decreasing. This chapter deals with the basic steps involved in the fabrication of devices. The purification process of silicon, crystal growth and wafer preparation are discussed first, followed by unit processes involved in fabrication. The process sequence to fabricate basic devices is described briefly at the end.

2.1 MATERIAL PREPARATION

As we have discussed in Section 1.1.1, most of the integrated circuits are fabricated with silicon. Therefore, our focus is on the fabrication of silicon devices. To fabricate devices, silicon must be in crystalline form without any defects. It must be extremely pure. Impurity of the order of a ppb (parts per billion) only is allowed.

2.1.1 Purification of Silicon

Silicon is abundantly available in nature in the form of SiO₂ (sand) which forms about 20% of earth's crust. Metallurgical Grade Silicon (MGS) is obtained by reduction of quartzite (a crystalline form of SiO₂ available in the form of rock) in a carbon arc furnace. From MGS Electronic Grade Silicon (EGS) is obtained by distillation process. EGS is polycrystalline in nature. It consists of impurities of the order of 1 ppb. (1 unwanted impurity per 1 billion or 10^9 silicon atoms).

2.1.2 Crystal Growth

This process is done to convert polycrystalline silicon to single crystalline silicon. Crystallisation takes place if molten silicon is allowed to solidify to a seed crystal. (Seed crystal is a highly pure single crystalline silicon which is used as the starting material for crystal growth). Two established processes used for crystal growth are:

- (1) Czochralski growth (CZ process) and
- (2) Float zone process (FZ process)

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Czochralski growth (CZ process): The set up for crystal growth by this method is shown in Fig. 2.1. The crystal is grown from EGS in molten state kept in a quartz lined graphite crucible. The melt is heated to a temperature of 1690K which is slightly greater than the melting point of silicon (1685K). The centre of the melt is at lowest temperature. The crystal growth is started by dipping a seed of single crystal silicon into the melt. The seed is suspended over the crucible by a holder attached to a rotating arm. The seed is Inserted into the melt by lowering the arm. As the bottom of the seed melts, the direction of motion of the arm is reversed. During this operation, the crucible is rotated to provide stirring and uniform heating of the melt. When the arm moves upward the melt in contact with the seed solidifies to form crystalline silicon with the structure of the seed, resulting in a larger crystal. The crystal growth stops when the crucible is depleted of melt.



Fig. 2.1 Czochralski crystallization process

To make p-type or n-type silicon, a precisely controlled quantity of Boron or Phosphorus is added to the melt. The concentration of impurity in the melt (liquid state) is usually less than that in the grown crystal (solid state). The ratio of concentration of impurities in the solid state (C_s) to the impurity in liquid state (C_l) at equilibrium is known as segregation constant (k_o)-

$$k_0 = \frac{C_s}{C_l} \tag{2.1}$$

The maximum concentration of impurities that can be introduced into a semiconductor at a given temperature T is known as *solid solubility*. Solid solubility increases with increase in temperature.

The oxygen content in crystal grown by CZ process is high (5 x 10^{17} to 2 x 10^{18} cm⁻³). This is due to the reaction of silicon in the melt with the quartz lining of crucible. This oxygen may become electrically active during subsequent process. Czochralski process is not used when material with resistivity more than 10 Ω cm is required.

Liquid encapsulated CZ method is used to grow GaAs. A molten dense layer of B_2O_3 floats over molten GaAs which prevents evaporation of As (which is highly volatile) from the melt.

Float zone process (FZ process): Float zone process uses an ultra pure rod of poly crystalline silicon (polysilicon). The rod is kept in vertical position by means of two chucks as shown in Fig. 2.2. This is enclosed in a chamber in which inert ambient is maintained by flow of Argon.



Fig. 2.2 Schematic of typical float zone apparatus

A single crystal seed is placed at the bottom of the polysilicon rod. The rod is heated from bottom to top by movable R.F coil. As the R.F coil moves up, the molten zone of the rod moves up and the lower portion solidifies and recrystallizes with the crystal structure of the seed. The molten zone is held together by the surface tension of the liquid. The desired impurity level (doping) can be obtained by using appropriately doped polysilicon rod.

The silicon crystal obtained by this process is superior to that in the CZ process because of the absence of crucible. Oxygen content is of the order of 10^{15} cm⁻³ only. Resistivities above 10 K Ω cm can be achieved. However, it is not possible to grow large diameter crystals using, this method.

Most of the impurities in Si and Ge have segregation constant less'than unity. Therefore, as the molten zone moves up and soldification continues most of the impurities are rejected from solid phase to liquid phase. As the molten zone reaches the top, impurities are collected at the top. Several runs of this process result in a crystal of desired purity and impurities collected at the upper end of the bar can be cut away. This process is called zone refining.

Example 2.1 A silicon crystal is to be grown by Czochralski process and is to contain 5 x 10^{15} boron atoms/cm³. Given $k_0 = 0.8$ for boron in Si, atomic weight of boron = 10.81 g/mole, density of silicon = 2.33 g/cm³. Avogadro number = 6.023 x 10^{23} atoms/mole.

a. Determine the initial concentration of boron atoms in the melt to produce the required density.

b. If initial amount of silicon in the crucible is 50 kg, how many grams of boron should be added.

Solution

a.

$$k_0 = \frac{C_s}{C_l}$$

C_s = 5x10¹⁵ atoms/ cm³
k₀ = 0.8
∴ C_l = $\frac{C_s}{k_0} = \frac{5 \times 10^{15}}{0.8} = 6.25 \times 10^{15} atoms / cm^3$

b. Weight of silicon =
$$50 \times 10^3$$
g

Volume of silicon =
$$\frac{weight}{density}$$

= $\frac{50 \times 10^3}{2.33}$ = 2.146×10⁴ cm³

Neglecting the change in volume on adding boron atoms

Number of boron atoms = Number of boron atoms/cm³
× Volume of Si
=
$$6.25 \times 10^{15} \times 2.146 \times 10^{4}$$

= 13.41×10^{19}
Weight of boron added = $\frac{\text{weight / mole}}{\text{atoms / mole}} \times \text{Total number of atoms}$
= $\frac{10.81}{6.023 \times 10^{23}} \times 13.41 \times 10^{19}$
= $2.40 \times 10^{-3} \text{ g}$
= 2.40 mg .

2.1.3 Crystal Slicing and Wafer Preparation

The crystal ingot has diameter upto 12 inches and length of 100 cm. This ingot is ground to an exactly cylindrical shape. A flat is ground at the end of the bar. A slice is cut from this end and the crystal orientation is determined by X-ray diffraction method. The slicing, is done at different angles until the desired orientation of the crystal at the surface is obtained.

The crystal is then cut into slices called wafers. Thickness of wafers vary from 0.4 to 1mm. The slicing is done by a ring shaped saw blade made of stainless steel. Diamond is bonded on the inner rim of the saw and cutting process is water cooled. About one third of the material is lost as saw dust.

The sliced crystal is subjected to two sided lapping under pressure with a mixture of Al_2O_3 and glycerine. Then, the wafers are subjected to chemical etching in mixture of HF, HNO₃ and acetic acid. One side of the wafer is then polished to mirror finish. Devices are fabricated on this wafer. Processing are done on the polished surface.

2.2 FABRICATION PROCESSES

The important unit processes involved in the fabrication of devices are

- 1. Oxidation 5. Isolation
- 2. Diffusion 6. Lithography
- 3. Ion implantation 7. Metallization
- 4. Epitaxy

The basic integrated circuit fabrication process is known as planar process in which introduction of impurities and metallic connections arc carried out from the top surface of the wafer. In planar process, several wafers consisting of similar devices or circuits can be processed simultaneously. Precise control of temperature, humidity and extremely clean environment are required for fabrication of devices.

2.2.1 Thermal Oxidation

Thermal oxidation of silicon is accomplished by placing the silicon wafers vertically in an open ended quartz tube. This quartz tube is placed in a resistance heated furnace at 900 to 1200° C. Dry oxygen or wet oxygen (oxygen + water vapour) may be used as the oxidizing agent. The reaction involved in oxide growth are as follows:

Si $+O_2 \rightarrow SiO_2$ (dry oxidation) Si $+ 2H_2O \rightarrow SiO_2 + 2H_2 \uparrow$ (wet oxidation)

The oxide growth rate is very low in dry oxidation. But, its electrical properties are excellent. Wet oxidation is much faster than dry oxidation. It is suitable for making thick oxides (exceeding $1\mu m$). But, it suffers from more structural defects and higher density of interface states.

When SiO_2 is grown on silicon wafer, thickness of silicon decreases as Si is consumed during oxidation. It can be shown that the ratio of thickness of silicon consumed to thickness of SiO_2 is 0.44 as illustrated in Example 2.2. A thermal oxidation system is shown in Fig. 2.3(a) and an oxide grown on silicon is shown in Fig. 2.3(b).



Fig. 2.3

Example 2.2 Determine the ratio of silicon consumed to the thickness of grown SiO₂ layer over the wafer. If a SiO₂ layer of 1000 A° is to be grown, what would be the thickness of used up silicon. Given, molecular weight of SiO₂ = 60.08 g/mole, density of SiO₂ = 2.20 g/cm³, atomic weight of Si = 28.09 g/mole, density of Si = 2.33 g/cm³

Solution

Volume of 1 mole of SiO₂ = $\frac{\text{molecular weight}}{\text{density}}$ = $\frac{60.08}{2.20} = 27.30 \text{ cm}^3$ Volume of 1 mole Si = $\frac{28.09}{2.33} = 12.055 \text{ cm}^3$ $\frac{\text{Volume of 1 mole of Si} \times \text{area}}{\text{Volume of 1 mole of SiO}_2 \times \text{area}}$ (1 mole of SiO₂ uses 1 mole of Si over the same area) $\frac{\text{thickness of silicon}}{\text{thickness of SiO}_2} = \frac{\text{volume of 1 mole of SiO}_2}{\text{volume of 1 mole of SiO}_2}$

$$=\frac{12.033}{27.30}=0.44$$

To grow 1000 A° of SiO₂, the thickness of used up silicon = $0.44 \times 1000 = 440$ A°. The thickness of oxide layer (t_{0x}) grown by thermal oxidation may be expressed as

$$t_{ox}^{2} + A \cdot t_{ox} = B(t + \tau)$$
(2.2)

where, A and B are constants whose values depend on the type of oxidation (wet or dry), temperature, crystal orientation of wafer, etc.

t is the time of oxidation and

 τ is initial fit parameter.

$$t_{0x} = \frac{A}{2} \left[\left(1 + \frac{t + \tau}{A^2 + 4B} \right)^{\frac{1}{2}} - 1 \right]$$

For very small thickness of oxide or short oxidation time t_{ox}^2 , term in equation (2.2) is negligible.

$$\therefore t_{ox} = \frac{B}{A}(t+\tau) \tag{2.3}$$

For thick oxides (long oxidation time) At_{ox} $\ll t_{ox}^2$

$$\therefore t_{ox}^{2} = B(t+\tau)$$

$$\therefore t_{ox} = \left[B(t+\tau)\right]^{1/2} \simeq \sqrt{Bt}$$
(2.4)

For small oxide thickness, t_{ox} is linearly proportional to time of oxidation (equation (2.3)). Therefore, B/A is called linear rate coefficient. For thicker oxides, the thickness has a parabolic relationship with time as given by equation (2.4). Therefore, B is called parabolic rate coefficient. A list of the values of these constants is given in table 2.1.

Oxidation temperature T ⁰ c	Dry oxidation			Wet oxidation		
	$B(\mu m^2/h)$	B/A (µm/h)	τ (h)	B (µm²/h)	B/A (µm/h)	τ (h)
800	0.0011	0.003	9	-	-	0
1000	0.012	0.071	0.37	0.29	1.27	0
1100	0.027	0.30	0.076	0.51	4.64	0
1200	0.045	1.120	0.027	0.72	14.40	0

Table 2.1 List of typical parameters of thermal oxidation

Example 2.3 A 1000 A thick SiO₂ layer is grown in dry oxygen at 1000⁰C, followed by 0.5 μ m thick oxide in wet oxygen at the same temperature. Determine the total time of oxidation. (At 1000⁰C, B = 0.012, B/A = 0.071, τ = 0.37 for dry oxidation and B = 0.29, B/A = 1.27 for wet oxidation)

Solution

$$t_{ox}^{2} + At_{0x} = B(t + \tau)$$
$$t = \frac{t_{ox}^{2}}{B} + \frac{t_{ox}}{B/A} - \tau$$

Time required to grow 1000 A° SiO₂ layer in dry oxygen = t_1 . $t_{ox} = 1000A=0.1 \mu m$

$$\mathbf{t}_1 = \left[\frac{(0.1)^2}{0.012} + \frac{0.1}{0.071} - 0.37\right]hr$$

Time required to grow the same thickness in wet oxidation $= t_2$

$$\mathbf{t}_2 = \left[\frac{(0.1)^2}{0.29} + \frac{0.1}{1.27}\right]hr$$

Time required to grow $(0.1 + 0.5)\mu m$ thick SiO₂ layer in wet oxidation = t₃.

$$t_{3} = \left[\frac{(0.6)^{2}}{0.29} + \frac{0.6}{1.27}\right]hr$$

= 1.71 hr
= 1.87+1.71- 0.113
= 3.467 hr
= 3 hr 28 min.

2.2.2 Diffusion

Total time required = $t_1 + t_3 - t_2$

This is a process of doping semiconductor wafer. Doping can be done selectively into silicon wafer by using SiO_2 as masking layer. This is possible because impurities like boron, phosphorus etc., do not diffuse through SiO_2 .

Diffusion process is usually done in two steps: pre- deposition and drive-in. In predeposition, a high concentration of dopant atoms are introduced at the silicon surface. This is done by transporting impurities in vapour form at temperature about 1000°C. At high temperature, the bonds in silicon atoms are broken and impurity atoms diffuse into the silicon wafer because of concentration gradient and replaces silicon atoms in the bond. Pre-deposition process produces a shallow, heavily doped layer. This is also known as constant source diffusion.

Drive-in process drives the impurities deep into the semiconductor. The source of impurity is removed after pre-deposition. Therefore, the total amount of impurity in the wafer (dose) remains constant during the drive-in process. This reduces the surface concentration and increases the junction depth. Drive-in diffusion is also called constant dose diffusion. Drive-in is done at a higher temperature (1000-1250°C) than pre-deposition.

Boron (acceptor impurity) and phosphorus (donor impurity) are the two common sources of impurities for diffusion in silicon. They have high diffusion rate in Si, low diffusion rate in SiO_2 and highly soluble in silicon. The profiles of impurities in pre-deposition and drive-in are shown in Fig. 2.4.



Fig. 2.4 n-impurity distributions into p-substrate, for pre-deposition and drive-in diffusion

A diffusion system is shown in Fig. 2.5. The wafers can be easily inserted into or taken away from the quartz tube as they are placed in a movable quartz boat (carrier). Impurities are introduced into the furnace in vapour form using N_2 and O_2 as carrier gases.



Fig. 2.5 Typical open-tube diffusion system

At high temperature $(1000^{\circ}C)$ these impurities diffuse into the silicon wafer. For drive-in process the supply of impurity is stopped and temperature is raised to $1100^{\circ}C$. The diffusion depth is decided by the precise control of temperature and time of diffusion.

Analysis of Diffusion Process

The diffusion process is governed by Fick's laws:

Fick's first law

$$\mathbf{J} = -\mathbf{D} \ \frac{\partial C(x,t)}{\partial x} \tag{2.5}$$

where

J is flux of material,

C(x, t) is dopant concentration at a depth x from the surface of wafer at time t, D is diffusion coefficient.

Fick's second law

$$\frac{\partial C(x,t)}{\partial t} = D \frac{\partial^2 C(x,t)}{\partial x^2}$$
(2.6)

Equation (2.6) is also known as diffusion equation.

Pre-deposition

The boundary conditions for pre-deposition are

$$\begin{split} &C(x,0)=0\\ &C(0,t_1)=C_s \mbox{ (Constant surface concentration)}\\ &C(\infty,t_1)=0 \end{split}$$

The solution of diffusion equation under these conditions is

$$C_1(x,t_1) = C_s \operatorname{erfc}\left[\frac{x}{2\sqrt{D_1 t_1}}\right]; \quad t_1 > 0$$
(2.7)

where erfc is complementary error function which is a tabulated function,

 D_1 is diffusivity (diffusion coefficient) of impurity at $T_1 \alpha e^{-K/T_1}$ where K is a constant.

 T_1 is temperature at which pre-deposition is done.

The dose of diffusion or the total impurities introduced during pre-deposition for a time t_1 is given by

$$Q_{\rm T}(t_1) = \int_0^\infty C_1(x, t_1) dx = \frac{2}{\sqrt{\pi}} C_S \sqrt{D_1 t_1}$$
(2.8)

Drive-in

This is the doping process with a constant dose Q_T. The boundary conditions are

$$C(\mathbf{x},0) = 0; \quad \mathbf{x} \neq 0$$
$$\frac{dC(0,t)}{dx} = 0$$

$$C(\infty, t_1) = 0$$
$$\int_{0}^{\infty} C_1(x, t_1) dx = Q_T \text{ constant.}$$

The solution of diffusion equation under these conditions is

$$C_2(\mathbf{x}, \mathbf{t}_2) = \frac{Q_T}{\sqrt{\pi D_2 t_2}} e^{-x^2/4D_2 t_2}$$
(2.9)

where

D₂ is diffusion coefficient of impurity at T₂

 T_2 is temperature at which drive-in is done and

t2 is drive-in time

This is a Gaussian profile, therefore drive-in diffusion is also called Gaussian diffusion.

Definition and Properties of Error Function

$$\operatorname{erf}(\mathbf{x}) = \frac{2}{\sqrt{\pi}} \int_{0}^{x} e^{-y^{2}} dy$$
$$\operatorname{erfc}(\mathbf{x}) = 1 - \operatorname{erf}(\mathbf{x})$$

where (error function) and erfc (error function complement) are tabulated functions.

$$erf(0) = 0$$

$$erf(\infty) = 1$$

$$\frac{d}{dx}erf(x) = \frac{2}{\sqrt{\pi}}e^{-x^2}$$

$$\int_{0}^{\infty} erfc(x)dx = \frac{1}{\sqrt{\pi}}$$

Example 2.4 After a pre-deposition step, it is found that 5×10^{15} phosphorus atoms cm⁻² are introduced in a p-type silicon sample doped with 10^{16} acceptor atoms cm⁻³. Calculate the junction depth when the drive-in diffusion is performed at 1200°C for two hours. D = 2.5×10^{-12} cm²/s at 1200°C.

Solution

Drive-in is a doping process with constant dose.

$$Q_T = 5 \times 10^{15} \text{ cm}^{-2}$$

Background doping $N_B = 10^{16}$ cm⁻³, $t = 2 \times 60 \times 60$ seconds.

The junction depth (x_j) is the distance from the surface of wafer where the dopant concentration equals the background doping (N_B) in the wafer.

From equation (2.9)

$$C_2(\mathbf{x},\mathbf{t}) = \frac{Q_T}{\sqrt{\pi Dt}} e^{-x^2/4Dt}$$

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when $x = x_i$

$$N_{B} = C_{2} (x_{j}, t) = \frac{Q_{T}}{\sqrt{\pi D t}} e^{-x_{j}^{2}/4Dt}$$

$$e^{-x_{j}^{2}/4Dt} = \frac{N_{B} \times \sqrt{\pi D t}}{Q_{T}}$$

$$x_{j} = \left(4Dt \ln \frac{Q_{T}}{N_{B}\sqrt{\pi D t}}\right)^{1/2}$$

$$= 4 \times 2.5 \times 10^{-12} \times 2 \times 60 \times 60$$

$$\left[\ln \frac{5 \times 10^{15}}{10^{16}\sqrt{\pi \times 2.5 \times 10^{-12} \times 2 \times 60 \times 60}}\right]^{1/2}$$

$$= 7.422 \times 10^{-4} \text{ cm}$$

$$= 7.42 \text{ µm.}$$

2.2.3 Ion Implantation

An alternate method for doping is to bombard selected area of the surface of the wafer with high energy impurity ions. These high energy ions can penetrate into the wafer. The faster the ions 'shot' at the wafer, the deeper they penetrate. On entering the wafer, due to collision with electrons and nuclei of silicon atoms, they lose their energy and stop penetration.

A simplified ion implantation setup is shown in Fig. 2.6. The ion source consists of the dopant material within a very strong electric field. This electric field is strong enough to separate the dopant molecules into constituent ions, forming a charged gaseous plasma. These charged ions are then accelerated to the desired velocity by control of the voltage along the accelerator tube. It is focused into a narrow beam of high velocity ions. The resulting ion current is of the order of 1 mA. The beam is turned through 90° by an analyzing magnet. This is done - to purify the beam of any unwanted ions which may also have been accelerated with the dopant beam. The magnetic field is so set up that only the desired dopant turns through right angle. Any other ion having different mass from that of the desired material is turned by a different angle.



Fig. 2.6 Ion implantation system

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The focused beam of dopant ions is then passed through X and Y scanning plates. The mechanism is almost identical to the scanning plates in a cathode ray oscilloscope which move the focused beam over the screen. In this case, the ion beam is moved over the target wafer, as the implantation has to be done bit by bit. (The whole wafer cannot be implanted in one operation).

The perpendicular distance from the semiconductor surface covered by the impurity atom before coming to rest is called projected range (R_p). The doping profile after ion implantation is given by

$$\mathbf{N}(\mathbf{x}) = \frac{Q_o}{\Delta R_p \sqrt{2\pi}} e^{-1/2 \left(\frac{z - R_p}{\Delta R_p}\right)}$$
(2.10)

N(x) = is dopant concentration at distance x from surface of wafer

 ΔR_p is standard deviation of projected range and

Q0 is total implantation dose (number of impurity ions per unit area)

$$Q_o = \frac{Jt}{q} \tag{2.11}$$

where

J is ion beam current density

t is implantation time

The peak implantation impurity concentration will be at $x = R_p$

$$\therefore N_p = \frac{Q_o}{\Delta R_p \sqrt{2}\pi}$$
(2.12)

Example 2.5 Phosphorus is implanted in a p-type silicon sample with a uniform doping concentration of 5×10^{16} atoms per cm³. If the beam current density is 2.5 μ .A per cm² and the implantation time is 8 minutes. Calculate the implantation dose. Assume $\Delta R_p = 0.3 \mu m$. Also find the peak impurity concentration.

Solution

$$\begin{split} J &= 2.5 \; \mu A/cm^2 = 2.5 \times 10^{-6} \; A/cm^2 \\ t &= 8 \; minutes = 8 \times 60 \; seconds \end{split}$$



Fig. 2.7 Implantation profile for boron in silicon for different values of ion-beam energy

Implantation dose $Q_o = \frac{Jt}{a}$

$$=\frac{2.5\times10^{-6}\times8\times60}{1.6\times10^{-19}}$$

= 7.5 × 10¹⁵ cm⁻²

Peak impurity concentration

$$V_{p} = \frac{Q_{o}}{\Delta R_{p} \sqrt{2\pi}}$$
$$= \frac{7.5 \times 10^{15}}{0.3 \times 10^{-4} \times \sqrt{2\pi}} = 9.97 \times 10^{19} \text{ cm}^{-3}$$

Ion implantation has the following advantages.

- (1) Doping levels can be precisely controlled, as it depends on the ion current.
- (2) The depth of dopants can be easily controlled.
- (3) Very shallow penetration is possible.
- (4) Extreme purity of dopant.
- (5) Uniform doping over the surface is possible.
- (6) Doping area can be precisely defined since the spread of the directed ion beam is very little.
- (7) As it is a low temperature process, the movement of impurities is minimum within the wafer.

The region near the surface of the wafer is subjected to mechanical damage due to implanting effect. The wafer is therefore subjected to an annealing process which consists of raising the temperature of the wafer to 800-1000° C for 20-30 minutes. This has two effects. Firstly, the semiconductor wafer can re-align its crystal structure, back to the single crystal which is important for efficient device operation. Secondly, it allows the dopant material to fit substitutionally into the crystal lattice.

2.22.4 Epitaxial Growth

Epitaxy is the process of growing a crystalline layer over a crystalline substrate. Epitaxially grown layer has same crystal structure as that of the substrate. When a material is grown epitaxially on a substrate of same material, the process is termed homo epitaxy, eg: Silicon grown on silicon. If layer and substrate are of different materials, the process is called hetero epitaxy, eg: A_1 Ga₁ - _xAs on GaAs.

By diffusion or ion implantation impurities (dopants) are driven into the semiconductor wafer. But in epitaxial growth a layer of doped semiconductor is grown (or deposited) over the existing semiconductor which may be of any doping. For example, it is not possible to form an n layer (light doping) on n^+ (heavily doped) semiconductor by diffusion or ion implantation. This can be easily achieved by epitaxial growth.

A simplified setup for growing epitaxial layer by chemical vapour deposition (CVD) is shown in Fig. 2.8. The process is known as chemical vapour deposition, as all the chemicals introduced and that take part in the reactions are in the form of gases. The silicon wafers are placed in a long boat shaped graphite crucible. The crucible is placed in a long cylindrical quartz tube with inlets and outlets for gases.

Two or more reactive gases are introduced into the chamber, one based on semiconductor material and one based on the dopant. The system is rf heated to a temperature of approximately

1200° C. The gases react in the heated chamber. This forms doped semiconductor and grows on the substrate. Any by-product gases are vented away from the chamber. The thickness of the layer varies from 3 to 30 microns. This type of epitaxial growth is called vapour phase epitaxy (VPE).



Fig. 2.8 Simplified setup for epitaxial growth

The following methods are also used for epitaxial growth. Liquid phase epitaxy (LPE) involves the substrate wafer being dipped into a melt consisting of semiconductor with a large amount of dopant material. This technique is used in the fabrication of hetero junction LEDs and lasers which are formed by ternary and quaternary compounds.

Molecular beam epitaxy (MBE) takes place in a very high vacuum chamber and consists of firing a beam of constituent atoms at the substrate. The beam sources most commonly used in MBE are Knudsen cells, electron beam sources and gas sources. The temperature is accurately controlled to maintain the required intensity of beam. The process is very slow, but control of the supply of epitaxial material is very good and very precise doping profiles can be achieved by this technique.

Organo-metallic vapour phase epitaxy (OMVPE) is another method used for epitaxial growth of compound semiconductors. Epitaxial growth of high quality GaAs layers can be obtained by the reaction between the organo-metallic compound trimethylgallium (TMG) with Arsine (AsH₃). The reaction takes place at a temperature of about 700°C. This growth method is widely used in the fabrication of solar cells and lasers. It is suitable for precise doping profiles and very thin layers.

2.2.5 Other Deposited Layers a. Deposited Oxide Layers

If silicon surface is covered with other layers, oxide must be deposited by chemical vapour deposition (CVD) process. There are number of options available for the reactive components. A mixture of silane and oxygen at 450° C may be used as the reactive component for deposition of a layer of SiO₂.

$$SiH_4 + 2O_2 \rightarrow SiO_2 + 2H_2O$$

b. Nitride Layers

Nitride layer finds use as an oxidation mask, high permittivity layer for capacitor structures, passivation layer against moisture and sodium ions, etc. Nitride layer can be deposited by CVD of ammonia with silane in the temperature range of 700-1000° C.

$$3SiH_4 + 4NH_3 \rightarrow Si_3N_4 + 12H_2 \uparrow$$

c. Polycrystalline Silicon

Polycrystalline silicon (or polysilicon) finds use as a substitute for epitaxial layer when the silicon surface is covered by another layer (metal or oxide). Heavily doped polysilicon is used as an interconnect material in multilevel metallization. It is also used for passivation, in undoped form. Added oxygen increases the resistivity further. Polysilicon is formed in a low pressure furnace at 600-650° C by pyrolysis of silane.

$$SiH_4 \rightarrow Si + 2H_2$$

2.2.6 Isolation

In integrated circuits isolation is required for the device to operate independently of the state of other devices. Different techniques are used for isolation. Some of them are (a) p-n junction isolation (b) dielectric isolation (c) Local oxidation of silicon.

Bipolar technology uses p-n junction isolation. A reverse-biased p-n junction isolates one device from another nearby device. The p^+ region extending from the surface to substrate as shown in Fig. 2.9 acts as isolation region. Devices may be made on n islands over the p-substrate. Junction isolation is simple and produces a planar isolation. The main disadvantage is parasitic capacitance of the collector substrate junction.



Fig. 2.9 p-n junction isolation

In dielectric isolation, V-groove is cut on Si surface and filled with insulator. The bottom of the wafer is ground upto the V-groove and the wafer is reversed. Now, islands of semiconductor appear over SiO_2 as shown in Fig. 2.10. This technique provides perfect isolation. This isolation technique is also known as silicon on insulator (SOI).



Fig. 2.10 Dielectric isolation process for forming silicon on insulator

The dielectric isolation is used in high voltage telecommunication IC's and for other high voltage and radiation hard digital applications. The main drawbacks of dielectric isolation are

- (1) The wafers are not as planar as normal starting material. (This affects further processes like lithography and vary silicon island thicknesses along the wafer)
- (2) The wafers made using this process are very expensive and
- (3) Isolation density is not very large.

Local oxidation of silicon or LOCOS is usually used to grow thick oxide on a silicon surface which already has a thin oxide on it. This enables a smooth transition from thick to thin oxide so that the surface remain almost planar. The thick oxide also acts as an isolation region from other devices. Fig. 2.11 illustrates the steps involved in local oxidation. This isolation technique is used in MOS devices.

Several other techniques such as trench isolation, side wall masked isolation (SWAMI), sealed interface local oxidation (SILO) etc., are also available.

Fig. 2.11 Cross-sectional views of a standard local oxidation of silicon (LOGOS) process

2.2.7 Masking and Lithography A. Production of Mask

In the fabrication of semiconductor devices, selective doping is often necessary i.e., certain regions of the wafer have to be protected against doping. This is usually done by covering the entire wafer by a protective layer (masking) and then removing this layer at selected regions of the wafer.

For most present-day IC's, the production of mask starts with a drawing, prepared with the aid of computer. The copies of the circuit pattern are photographically reduced until they are ten times the actual size. A step and repeat camera with a reduction factor of 10 is used to make the final mask. Rows and columns of identical images are transferal to a glass plate called a master. The primary mask is used to make working copies using photosensitive glass plates. These copies called **reticles** are then used for actual image transfer to a semiconductor wafer.

b. Lithography

Lithography transfers the desired patterns to the surface of the wafer. Lithographic technique is a limiting factor which decides the resolution and feature size in IC fabrication. It is also the most complicated and expensive process in microelectronic fabrication.

c. Photolithography

The photolithographic process "involves the transfer of the image from the mask to the surface of the wafer by the use of UV light and a photoresist. Photoresists are chemical compositions containing light sensitive material. They come in liquid form. There are two types of photoresists: negative and positive. Exposure to UV light hardens a negative photoresist and therefore the exposed resist becomes insoluble in a developer solution while the unexposed resist is soluble. A positive resist becomes soft when exposed to UV light. As a result, the exposed resist dissolves in the developer and unexposed resist remains insoluble. The sensitivity of positive resist is less than that of a negative resist.

The application of thin film of photoresist over the wafer is achieved by placing a small drop of resist on the top of the wafer and then spinning the wafer at high speed. This results in a very thin, even layer of liquid resist over the wafer surface. The wafer is then baked at 100°C in an oven to remove the excess solvent (prebaking). After cooling to room temperature, the wafer is exposed to UV light through the mask and then developed in a developer. It is again baked in an oven (postbaking) to increase the adherence of the resist to the surface of the wafer.

Fig. 2.12 illustrates the steps involved in photolithographic process.

The process sequence for selective diffusion by photolithography is listed below:

- 1. Grow oxide
- 2. Coat photoresist
- 3. Postbake
- 4. Prebake

8. Etch oxide to open window

6. Remove photoresist from exposed portion

9. Strip photoresist

7. Postbake

5. Place reticle (mask) over photoresist 10. Diffuse impurity through window.

There are many methods of photoresist exposure through a mask. The simplest method is contact printing in which the mask remains in contact with the photoresist. But if there are particles protruding from the wafer surface, the mask is locally damaged by them. Proximity printing partially overcome this problem. In proximity printing, the mask is separated from the wafer by a small distance of about 20 μ m. Another solution for mask damage problem is

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projection printing in which the mask is separated from the wafer, and its image is projected on the surface of the wafer using an optical system.

Fig. 2.12 Selective diffusion by photolithography

Diffraction effects limit the line width that can be obtained using UV light. The practical limit of contact printing and projection printing with UV light is reached at a line width of about 1 to 2 μ m. Because of diffraction effects, optical lithography is not capable of being extended to feature size much less than 0.2 μ m. If smaller features are to be imaged, the diffraction effects have to be reduced by using shorter wavelength radiations like X-rays or an electron beam.

Electron-beam lithography (EBL)

Electron beam lithography is used to generate feature size less than 1 μ m. Two types of E-beam systems in use are E-beam pattern generator and E-beam projection system. In E-beam., the energy required to effect the desired chemical change after exposure is given by electrons. EBL has demonstrated the ability to produce feature sizes of about 100 Å, but the process is too slow. The resolution that can be achieved in E-beam exposure is limited by the scattering of high energy electrons entering the resist. These electrons cause blurring of image in the resist.

X-ray lithography

X-ray lithography is similar to optical lithography except that X-rays are used instead of UV light. The exposure of the resist on the wafer is performed by proximity printing, keeping a gap of 25 to 40 μ m between the wafer and the mask. The short wavelength of X-ray reduces diffraction effects leading to high image quality with sharp edges. X-ray lithography has the potential for volume production since it is a parallel process. Feature size upto 0.1 μ m can be achieved by X-ray lithography. But, serious issues like mask distortion and aging are faced by X-ray lithography at submicron feature size.

2.2.8 Pattern Definition

After a photoresist image has been formed on the surface of the wafer, next process involves transferring that image into a layer under the. resist. This is done by selective removal of material from the unmasked regions. The technique by which material can be uniformly or selectively removed is called etching. Photolithegraphy is also used for patterning the metal and other layers. Some of the etching techniques used are wet chemical etching, plasma etching and reactive ion etching.

a. Wet etching

This method involves the immersion of the wafer in the etching solution at a predetermined temperature to form soluble by-products. Many solutions are available for the selective etching of different materials. SiO₂ is etched in a buffered solution of HF and NH₄F. Si₃N₄ is etched in H₃PO₄ at 140-200°C. Wet etching is also used to pattern metal lines. A common etchant for Al is 77% of H₃PO₄, 3% HNO₃ and 20% acetic acid. The etch time is determined by the etching rate of the solution. The main problem with wet etching is undercutting. Undercutting is the lateral extent of the etch under the photoresist mask. Undercutting limits the use of wet chemical etching to devices with dimensions larger than 15 µm.

b. Plasma etching

Plasma etching is a dry etching process in which reactive gases are fed into a reaction chamber. This is excited by high strength RF field to form a plasma of charged ions. These ions react with the material to be etched which evaporate off from the wafer. CF_4 is the commonly used compound for etching Si, SiO₂ and Si₃N₄. Plasma etching has several advantages over wet chemical etching. Plasmas are much easier to start and stop than wet etching. Plasma etch processes are much less sensitive to small changes in the temperature of the wafer. These two factors make plasma etching more repeatable than wet etching. There is less undercutting and definition of pattern is better in the case of plasma etching. Also, plasma etch process produces less chemical waste than wet etching process.

c. Reactive ion etching

In reactive ion etching, the wafers to be etched are kept in the electric field between two parallel plates in a reactor and a plasma is produced between these plates. Etching takes place partly by reaction of the ions with the etched layer and partly by removal of material by ion bombardment. The etching rate depends on the gas pressure in the reactor and the sample geometry. Undercutting is controlled but radiation damage is introduced in the substrate, particularly when etching SiO_2 over Si.

2.2.9 Metallisation and Interconnection

In an integrated circuit, different devices on the chip are to be interconnected. Metallic connection is also required for external connecting leads. The resistance of interconnecting metals must be very low to minimize voltage drop in the lines and to reduce the delay time. The connection must also be an ohmic contact. (An ohmic contact is a connection between semiconductor and metal which conducts well in both directions or very low resistance in both directions of conduction.) Aluminium is the obvious choice for ohmic contact with silicon due to the following reasons.

- (1) It has high conductivity.
- (2) It is easy to evaporate Al.
- (3) Easy to etch.
- (4) Low cost.
- (5) Adheres well to Si and SiO_2 .
- (6) Do not introduce undesirable levels in the bandgap as in the case of copper or gold.
- (7) It is non-corroding.

Some of the methods used for depositing aluminium on silicon substrate are resistance heating, electron beam heating and sputtering.

Resistance heating

In this method the source and silicon substrate are placed in an evacuated chamber. The source is usually a small piece of aluminium attached to a coil of tungsten. The tungsten coil acts, as a heater. On heating, aluminium evaporates and the Al molecules travel to the substrate where they condense to form a thin layer over the entire wafer surface. The aluminium film is removed from unwanted portion by etching with phosphoric acid or by dry etching with appropriate mask. A typical aluminium interconnection is shown in Fig. 2.13.

Fig. 2.13 An aluminum interconnection between two diffused silicon regions

Electron beam heating

In this method aluminium is placed in a crucible kept in a vacuum chamber. The wafers are also placed in the same chamber. Aluminium is subjected to a high intensity electron beam ejected by an electron gun. The electron beam vapourizes aluminium which travels to the wafer forming a thin layer. By masking and photolithography the desired metallization pattern is formed on the wafer.

Sputtering

The material to be deposited is placed in a container filled with inert gas and maintained, at low pressure. The substrate is also placed in the same container. The wafer acts as the anode and material to be deposited as cathode. A high voltage radio frequency is applied between anode and cathode, which ionizes the inert gas in the chamber. The positive iocs are accelerated to Al which acts as cathode. On collision with these ions, aluminium gets vapourized. A gas of aluminium atoms is generated and deposited on the surface of the wafer. After deposition the wafers are placed in a furnace so that Al gets bonded to the surface of the wafer.

The interconnections between elements of an integrated circuit are made by aluminium lines having a thickness of about 0.5 μ m. These are laid on the top of the SiO₂ layers which covers the wafer surface. Openings are made in the SiO₂ layer by photolithography, so that aluminium layer is connected to silicon to form ohmic contact.

Very complicated integrated circuits have two or three vertically stacked layers of interconnections separated by SiO_2 layers (multi layer metallization). The interconnecting lines terminate at the aluminium pads from which connections to outside are made. The connections from chips to external leads are produced by the metallization pattern around the periphery ofthe chip known as bonding pads. The bonding pads are connected by wires to the package. These pads are about 100 µm square and the connecting wire of diameter of about 25 µm is made of gold. Fig. 2.14 shows typical bonding pads and connections to external leads of an IC.

2.3 FABRICATION PROCESS SEQUENCE FOR BASIC DEVICES

This section describes the process sequence to fabricate basic devices such as diodes. BJT, CMOS, resistors and capacitors.

Fig. 2.14 Typical bonding pads and connection to external leads

2.3.1 Sequence of Diode Fabrication

Fig 2 15 illustrates the fabrication of many isolated p-n junctions on a single wafer which is nfype. Boron is selectively diffused to form p-n junction. Individual devices can be separated by scribing and breaking the wafer. The individual devices are mounted on appropriate packages and leads are connected to the aluminum contact.

Fig. 2.15 Fabrication steps of a p-n junction diode

2.3.2 Sequence of Discrete BJT Fabrication

The most common type of bipolar devices used in ICs is the n-p-n transistor. The process sequence for its fabrication is shown schematically in Fig. 2.16.

The starting material for the process is an n-type silicon wafer. An oxide layer is grown uniformly on the wafer and subsequently photolithography is done to open a window. The sample is placed in a furnace for boron diffusion, forming the p-type base region. After re-oxidation a new window is opened in the oxide for phosphorus diffusion forming n^+ emitter region. After opening windows to the top surface of p and n+ regions, aluminium is evaporated onto the wafer. The final metallization pattern is defined by photolithography and the unwanted Al is etched away.

Several thousands of such transistors can be made on a single wafer of Si and then separated by scribing and breaking into individual devices. The n-type substrate is alloyed to a header to provide contact to collector region. Gold or aluminium wires are bonded to the metalized regions to provide leads to the emitter and base. The final encapsulation is done by a hermetically sealed header or a molded plastic case, depending on the power rating and environmental specifications.

Fig. 2.16 Steps in fabrication of n-p-n transistor

2.3.3 Sequence of CMOS Fabrication

CMOS is the dominant semiconductor technology today due to very low power dissipation, increased density and reduced cost. A common classification of CMOS process is by the kind of subtrate used: n-well, p-well or twin well (tub). In a CMOS process, both n-channel and p-channel MOSFETs are fabricated. Either the n-type wafer is selectively doped p-type to create a p-well or a n-well is created in a p-type wafer. If both types of wells are created, the process is called twin tub (well) process.

The process sequence to realize CMOS inverter shown in Fig. 2.17 by n-well process is shown in Fig. 2.18.

Steps involved in the process are as follows:

Step 1: Using mask 1 define n-well region by growing oxide and etching window in the oxide. Implant Arsenic through the window to form n-well (Fig. 2.18(a)).

Step 2: Define active region (region consisting of source, drain and gate of n-MOS and p-MOS) by mask 2 and grow oxide in regions outside the active area by local oxidation which acts as the Field oxide (FOX). [Fig. 2.18(b)].

Step 3: Grow gate oxide by dry oxidation and deposit polysilicon over it. Dope polysilicon with arsenic and pattern it using mask 3. [Fig. 2.18(c)].

Step 4: Implant n-MOS source-drain regions. Polysilicon formed by step 3 prevents n-MOS source and drain regions extending into the channel region. [Fig. 2.18(d)].

Step 5: Similar to step 4 implant p-MOS source and drain regions. [Fig. 2.18(e)].

Step 6: Deposit phosphosilicate glass and etch windows for metal contacts. [Fig. 2.18(f)].

Step 7: Deposit metal and pattern it using mask 7. [Fig. 2.18(g)].

Step 8: Deposit silicon nitride as a passivation layer. Again lithography is done for bonding pads.

Fig. 2.17 CMOS inverter

2.3. 4 Fabrication of Resistors

Resistors in integrated circuits are made by impurities diffused into a semiconductor of opposite type. Fig. 2.19(a) shows a resistor fabricated by p-diffusion in n-substrate. This diffusion may be performed simultaneously with base diffusion. Metallic contacts are made at two ends of the resistor as shown in Fig. 2.19(a).

If *L* is the length, W-width, t-thickness of the layer and ρ is the average resistivity of the layer in Ω cm then, resistance (R) of the layer is given by

$$\mathbf{R} = \frac{\rho L}{Wt} \tag{2.13}$$

Fig. 2.18 Process sequence to fabricate CMOS inverter by n-well technology

The resistance of a square of the material (W = L) is called sheet resistance, its unit being ohms per square. Sheet resistance

$$R_{s} = \frac{\rho}{t} (Q \ L = W)$$

$$R = R_{s} \frac{L}{W}$$
(2.14)

Or

Where $\frac{L}{W}$ is called the aspect ratio.

In order to obtain high value of R, W is made as small as possible within the requirements of heat dissipation and photolithographic resolution. To reduce the amount of space used for resistors and to obtain high resistance values surface layers with high sheet resistance are necessary. Ion implantation is used to form shallow regions of very high sheet resistance. Ion implanted resistors allow considerable reduction in chip area and are especially suited for low-power digital and linear micro circuits. To realise very high value resistors, meander patterns are usually used.

2.3.5 Fabrication of Capacitors

Junction capacitors and dielectric (MOS) capacitors are the commonly used capacitors in monolithic circuits. Junction capacitors are made by using capacitance formed between p and n regions of a reverse-biased diode.

The main drawbacks of junction capacitor are their bias dependence and finite leakage current through the junction. Voltage independent capacitors are obtained using MOS structures. The cross-sectional views of a p-n junction capacitor and MOS capacitor are shown in Fig. 2.20(a) and (b).

(a) Cross-sectional view of p-n junction capacitor

(b) Cross-sectional view of MOS capacitor

Fig. 2.20

Solved Problems

Problem 2.1

A silicon crystal is to be pulled from the melt and doped with phosphorus. If Si weighs 1 kg, how many grams of phosphorus should be introduced to achieve a donor concentration of 2 x 10^{15} cm⁻³ during initial growth, k_o for P in Si is 0.32, atomic weight of P = 30.97 g/mole and density of Si 2.53 g/cm³

Solution

$$k_0 = \frac{C_s}{C_l}$$

$$C_s = 2 \ge 10^{15} \text{cm}^{-3}; \ k_0 = 0.32$$

$$\therefore C_l = \frac{2 \times 10^{15}}{0.32} = 6.25 \times 10^{15} \text{ cm}^{-3}$$
Weight of silicon = 1 kg = 1000g
Density of silicon = 2.53 g/cm^3
Volume of 1 kg of Si = $\frac{1000}{2.53} = 395.26 \text{ cm}^3$
Number of phosphorus atoms in the melt = $C_l \times$ Volume of silicon
(Change in volume due to addition of phosphorus is neglected)
= $6.25 \ge 10^{15} \ge 395.26$
= $2.47 \ge 10^{15} \ge 395.26$
= $2.47 \ge 10^{18}$
Atomic weight of phosphorus = 30.97 g/mole
i.e., weight of $6.023 \ge 10^{23}$ atoms = 30.97

:. Weight of 2.47 x
$$10^{18}$$
 P atoms = $\frac{30.97}{6.023 \times 10^{23}} 2.47 \times 10^{18}$
= 1.27 x 10^{-4} g
= 0.127 mg.

Problem 2.2

A silicon sample is covered with 0.25 μ m thick SiO₂ layer. Find the time required to grow an additional 0.20 / μ m thick SiO₂.layer at 1200°C by dry oxidation (B = 0.045, B/A = 1.120, τ = 0.027)

Solution

Time required to grow 0.25 μ m thick oxide in dry oxygen at 1000C = t₁,

$$t_{1} = \frac{t_{0x}^{2}}{B} + \frac{t_{0x}^{2}}{B/A} - \tau$$
$$= \frac{(0.25)^{2}}{0.045} + \frac{0.25}{1.120} - 0.027$$
$$= 1.58 \text{ hr}$$

Time required to grow (0.25 + 0.20) μ m thick oxide in dry oxygen at 1200^oC = t₂

$$t_2 = \frac{(0.45)^2}{0.045} + \frac{0.45}{1.120} - 0.027$$

Therefore time required to grow additional 0.25 μ m thick oxide layer = t₂ - t₁ 4.87 - 1.58 = 3.29 hr.

Problem 2.3

A SiO₂ layer is grown by wet oxidation at 1000° C for 40 minutes followed by 1 hr dry oxidation at 1200° C. Determine the thickness of the oxide layer formed. B = 0.29, B/A == 1.27 for wet oxidation at 1000° C, B = 0.045, B/A = 1.12 and τ = 0.027 for dry oxidation at 1200° C. Thickness of oxide grown by wet oxidation

$$t_{0x} = \frac{A}{2} \left[\left(1 + \frac{t + \tau}{A^2 / AB} \right)^{\frac{1}{2}} - 1 \right]$$

B=0.29, B/A =1.27 \therefore A = 0.228 t=40 minutes = 40/60 hr = 0.667 hr, $\tau = 0$

$$\therefore t_{0x} = \frac{0.228}{2} \left[\left(1 + \frac{0.667}{\frac{(0.228)^2}{4 \times 0.209}} \right)^{\frac{1}{2}} - 1 \right]$$

 $= 0.340 \mu m$

Time required to grow 0.340 μ m thick oxide by dry oxidation at 1200^oC is

$$t = \frac{t_{0x}^2}{B} + \frac{t_{0x}}{B/A} - \tau$$

B = 0.045, B/A =1.12, $\tau = 0.027$
$$t = \frac{(0.45)^2}{0.045} + \frac{0.45}{1.120} - 0.027$$

= 2.84 hr

Thickness of oxide layer obtained in (2.84 + 1) hr is

 $\mathbf{t}_{ox} = \sqrt{\mathbf{B}(\mathbf{t} + \tau)} \left(\therefore A t_{ox} \ll t_{ox}^2 \text{ for long oxidation times} \right)$

$$= \sqrt{0.045(3.84 + 0.027)}$$

= 0.417 µm.

Problem 2.4

In the diffusion process, Q is defined as the total number of atoms per unit area of the semiconductor.

$$Q = \int_{0}^{\infty} C(x,t) dx \text{ where } C(x,t) = C_{\text{serfc}} \left(\frac{x}{2\sqrt{Dt}} \right)$$

Use the equation for the pre-deposition concentrations to determine an expression for B in terms of D, t and $C_{\rm s}$

Solution

$$Q = \int_{0}^{\infty} C(x,t) dx$$
$$= \int_{0}^{\infty} C_{s} erfc\left(\frac{x}{2\sqrt{Dt}}\right) dx = C_{s} \int_{0}^{\infty} erfc\left(\frac{x}{2\sqrt{Dt}}\right) dx$$

Let

$$\frac{x}{2\sqrt{Dt}} = y$$

$$dx = 2\sqrt{Dt}dy$$

$$\therefore Q = C_s \int_0^{\infty} erfcy. 2\sqrt{Dt}dy$$

$$= C_s 2\sqrt{Dt} \int_0^{\infty} erfc.ydy$$

$$= C_s 2\sqrt{Dt} \times \frac{1}{\sqrt{\pi}} \left(Q \int_0^{\infty} erfc.ydy = \frac{1}{\sqrt{\pi}} \right)$$

$$= \frac{2}{\sqrt{\pi}} C_s \sqrt{Dt}$$

Problem 2.5

For a 100Ω /square diffusion, find the aspect ratio for a $5k\Omega$ resistor and draw a diffusion pattern for a width of $10\mu m$.

Solution

$$\mathbf{R} = \mathbf{R}_{\mathrm{s}} \frac{L}{W}$$

R_s is sheet resistance = 100Ω /square R in 5kΩ ∴ Aspect ratio $\frac{L}{W} = \frac{5000}{100} = 50$

$$\frac{W}{W} = \frac{100}{100} = 30$$
$$W = 10 \mu m$$
$$\therefore L = 500 \mu m$$

Points to Remember

- Crystal growth is the technique by which single crystalline semiconductor material is grown from a melt of highly pure poly crystalline semiconductor material. The two crystal growth techniques are Czochralski growth and float zone process.
- Segregation constant (k_o) is the ratio of impurities in solid state to liquid state.

$$k_0 = \frac{C_s}{C_l}$$

- Solid solubility is the maximum concentration of impurities that can be introduced into a semiconductor at a given temperature.
- The important steps involved in fabrication are:
- (a) Oxidation: It is the process of growing or depositing oxide, usually done at high temperature (900-1200^oC).

Thickness of thermally grown oxide is governed by the equation

$$t_{0x}^2 + At_{0x} = B(t+\tau)$$

For thick oxides (large oxidation time) $t_{ox} \simeq \sqrt{Bt}$

For thin oxides (small oxidation time) $t_{ox} \simeq \frac{B}{A}(t+\tau)$

- (b) Diffusion: It is a method of doping a semiconductor wafer by introducing gaseous impurities at high temperature. Diffusion is done in two steps: pre-deposition and drivein
 - i. pre-deposition introduces a high concentration of impurities near the surface,

ii. drive-in process drives the deposited impurities deep into the wafer.

For pre-deposition: Impurity profile is

$$\mathbf{C}_{1}(\mathbf{x},\mathbf{t}_{1}) = \mathbf{C}_{\text{serfc}} \left[\frac{x}{2\sqrt{D_{1}t_{1}}} \right]; \mathbf{t}_{1} > 0$$

and dose of diffusion (total quantity of impurity introduced into the wafer)

$$Q_T = \frac{2}{\sqrt{\pi}} C_s \sqrt{D_1 t_1}$$

For drive-in

$$C_{2}(x,t_{2}) = \frac{2C_{s}}{\sqrt{\pi}} \sqrt{\frac{D_{1}t_{1}}{D_{2}t_{2}}} e^{-x^{2}/4D_{2}t_{2}}$$

(c) Ion implantation is a low temperature doping process in which dose and depth can be precisely controlled.

Implanted impurity profile for ion integration is

$$N(x) = \frac{Q_0}{\Delta R_p \sqrt{2\pi}} e^{-1/2 \left(\frac{x - R_p}{\Delta R_p}\right)}$$

Dose
$$Q_0 = \frac{Jt}{q}$$

- (d) Epitaxial growth is the process of growing a layer of semiconductor of identical crystal structure and of any doping over a semiconductor wafer.
- (e) Isolation is used to isolate devices on a wafer, p-n junction isolation is used in bi-polar technology. LOCOS is used in MOS technology.
- (f) Lithography is used to transfer the desired patterns to the surface of the wafer. Processes usually used are photo-lithography, electron beam lithography and X-ray lithography.
- (g) Pattern definition is done by etching which is a technique by which material can be uniformly or selectively removed to form required pattern on the wafer surface. Some of the etching techniques are wet etching, plasma etching, reactive ion etching.
- (h) Metallization and interconnection: Different devices on the 1C chip are interconnected by metallization with Al, connected to bonding pads by gold wires and bonded to external leads on the packet.

<u>Exercise Problems</u>

- (1) A semiconductor crystal with acceptor concentration $N_A=2 \times 10^{16} \text{ cm}^{-3}$ must be obtained by Czochralski technique. What weight of boron must be added to the melt if it contains 10 kg of silicon. Assume $k_0 = 0.8$ for B in Si.
 - **Ans:** 1.925 mg.
- (2) Oxidation of Si crystal is performed at atmospheric pressure and 1373 K for a duration of 1 hr. Compute the thickness of the oxide layer for
 - (a) Dry oxidation in O₂ atmosphere,
 - (b) Wet oxidation.

```
Ans: 0.131 μm (b) 0.661 μm
```

- (3) A Si surface, partially covered by a SiO₂ layer of 0.5 μm thickness is further oxidised by wet process at 1373 K for 2 hrs. Compute the thickness of the resulting oxide layer (a) Over the exposed Si area and
 - (b) Over the area originally covered by the $0.5 \mu m$ oxide layer. Comment on the result.

Ans: (a) 0.956 μm (b) 1.09 μm.

- (4) A layer of gate oxide of thickness 0.5 μ m is to be grown on a Si surface. Oxidation is to occur at 1200°C.
 - (a) Is dry or wet oxidation preferable?
 - (b) How deeply will the oxide penetrate below the original Si surface.
 - (c) What is the duration of oxidation.

Ans: (b) 0.22 µm (c) 5.975 Hrs.

- (5) Pre deposition of boron in a Si sample doped with 10¹⁷ As atoms/cm³ has a duration of 3 minutes at 1200°C. Compute ',
 - (a) Net doping at $0.8 \mu m$ from-the surface

(b) The junction depth; $D = 10^{-12} \text{ cm}^2/\text{s}$, $C_s = 2.3 \text{ x} 10^{20} \text{ cm}^{-2}$.

Ans: (a) $5.75 \times 10^{15} \text{ cm}^{-3}$ (b) $0.668 \mu \text{m}$.

(6) After pre-deposition, the semiconductor specimen of Example 5 undergoes drive-in diffusion at 1100°C for 4 hrs. Compute

- (a) Surface concentration of the diffused species
- (b) Impurity dose
- (c) Junction depth after drive in diffusion

(d) The back ground doping that would be required to drive the junction depth to 2 μ m after driver- in diffusion. Diffusion constant D at this temperature is 1.7 x 10⁻¹³ cm²/s.

Ans: (a) $3.97 \times 10^{19} \text{ cm}^{-2}$ (b) $3.48 \times 10^{15}/\text{cm}$

- (c) 2.42 μ m (d) 6.679×10¹⁶ cm⁻³.
- (7) Boron is diffused at a temperature 1100^oC with a constant surface concentration of 3 x 10¹⁹ cm⁻³ on a uniformly doped n-type Si sample of resistivity 5 Ω cm at 300 K. How long should the diffusion be carried out to obtain a junction depth of 5 μ m. n_i at 300 K is 1.5 x 10¹⁰ cm⁻³; μ n = 1300 cm²/Vs, and D = 1.7 x 10⁻¹³ cm/s.
 - Ans: 11.815 Hrs.
- (8) An n-type silicon sample with a background concentration of 2x 10¹⁵/cm³ is implanted with boron at 100 k eV.

(a) If the target area is 100 cm² and the beam current is 1 mA calculate the duration of implantation to realize a dose of 5 x 10^{15} cm².

(b) Assuming $R_p = 0.3 \ \mu m$ and $\Delta R_p = 0.3 R_p$. Calculate the junction depth and peak doping concentration.

Ans: (a) 80 s (b) 1.976 μm , 1.376 μm.

<u>Review Questions</u>

- (1) How is semiconductor material processed before its crystal growth?
- (2) Explain the different crystal growth techniques.
- (3) Compare float zone process and Czochralski process.
- (4) What is zone-refining?
- (5) What is wafer?
- (6) How is crystal ingot converted to wafers?
- (7) What are the unit processes involved in the fabrication of integrated circuits?
- (8) What is meant by .dry oxidation and wet oxidation? Compare the features of oxide grown by dry and wet oxidations.
- (9) What is the equation governing oxide thickness? Explain.
- (10) What do you mean by linear and parabolic rate coefficients?
- (11) Write the expression for thickness of thin and thick oxides in terms of oxidation time and rate coefficients.
- (12) Explain with diagram a typical oxidation system.
- (13) What is the difference between pre-deposition and drive-in?
- (14) Give the expressions for doping profile and dose of impurities in pre deposition.
- (15) Write the expression for doping profile in drive-in (Gaussian) diffusion.
- (16) Compare ion-implantation with diffusion.
- (17) Explain with diagram a typical diffusion system.
- (18) Write the expression for doping profile in ion implantation and implantation dose? Explain.
- (19) What is epitaxial growth? Discuss the different techniques used to grow epitaxial layer.
- (20) Explain with diagram a typical vapour phase epitaxial growth system.
- (21) What are the different deposited layers used in fabrication process? Briefly explain.

- (22) Why is isolation needed in integrated circuits?
- (23) Explain p-n junction isolation with diagram. What are its features?
- (24) Explain LOCOS process with a neat diagram.
- (25) Explain with diagram silicon on insulator (SOI).
- (26) What is meant by lithography?
- (27) What are the different methods of lithography? Compare their features.
- (28) Explain with neat diagram different lithographic steps involved in selective diffusion over a wafer.
- (29) What is meant by pattern definition?
- (30) Explain briefly the different techniques used for etching.
- (31) What are the common etchants used for etching the following:
- (a) SiO_2 (b)Al (c) Si (d) Si_3N_4
- (32) What is meant by undercutting?
- (33) Why is aluminium preferred for metallization?
- (34) Explain metallization and interconnection procedure with diagrams.
- (35) Explain with the help of diagrams typical process sequences to fabricate p-n junction.
- (36) Explain process sequence to fabricate a discrete BJT.
- (37) Explain fabrication sequence of n-well C-MOS process.
- (38) Explain fabrication sequence of p-well C-MOS process.
- (39) How are resistors fabricated in integrated circuits?
- (40) What is meant by sheet resistance? How is IC resistance (R) related to sheet resistance?
- (41) What are the types of capacitors used in integrated circuits? Draw the cross-sectional view of each.