College of Engineering Trivandrum, Thiruvananthapuram

P4/6078/21/CET 24.09.2021

NOTICE INVITING TENDER

Tender No.	:16/2021/P4/CET/ECE
E tender ID	: 2021_DTE_443225_1
Superscription	:Purchase of FPGA Trainer kit for Digital Lab of Electronics & Communication Department
Last date and time of receipt of tender on the website (www.etenders.gov.in)	:20/10/2021 2 P.M
Date and time of opening of tender	22/10/2021 2 P.M
Date upto which the rates are to be firm	25/04/2022
Tender Cost	:₹826/-
EMD required	:₹3200/-
Address of the officer to whom hardcopy is to be send.	:THE PRINCIPAL,COLLEGE OF ENGINEERING TRIVANDRUM, THIRUVANANTHAPURAM-695016, KERALA :GSTIN :32AAAGC0358L1ZP

Specifications are attached as Annexure.

General conditions

1. The unit price, all other charges such as delivery, transporting, packing, shipping, loading and unloading charges etc, and GST must be shown separately and should be furnished unambiguously.
2. Payment : 100% after the successful supply, installation, and satisfactory performance.
3. Delivery Period: Maximam Delivery period will be 60 days from the date of receipt of supply order.
4. For : ***Electronics & Communication Engineering*** Department of this institution.
5. Warranty: 1 year warranty and
6. Agreements as per NIT 2 in Rs.220/- Kerala Stamp Paper and tender form should be uploaded.
7. 5% security deposit along with agreement should be furnished within a month/fortnight from the date of receipt of supply order.
8. Date of opening of tender : In case the proposed date declared is holiday, the tender will be opened on the next working day.
9. Only GST registered firm can participate in the tender. GST number must be mentioned. The firm under composition scheme must mention the words "Composition taxable person" in their documents and should submit proof for that.
10. After E-Tendering the hard copy of the agreement should submit to the undersigned before the

date of opening of the tender.

11 GST 18%

NB: The Tender procedure will be made as per Rules mentioned in the Revised Store Purchase Manual.

The bidders should participate this tender through E-Tendering System. Tender cost and EMD should be submitted only through online. For more details Contact Ph. 0471 2577088, 0471 2577188, 0471 2577388,0471 2515760.

Specifications

NAME OF COMPONENTS	Quantity
FPGA Trainer Kit (·33,280 logic cells in 5200 slices (each slice contains four 6-input LUTs and 8 flip-flops)· 1,800 Kbits of fast block RAM· Five clock management tiles, each with a phase-locked loop (PLL)· 90 DSP slices· Internal clock speeds exceeding 450MHz· On-chip analog-to-digital converter (XADC) ·16 user switches · 16 user LEDs · 5 user pushbuttons · 4-digit 7-segment display · 4 Pmod connectors o 3 Standard 12 pin Pmod o 1 dual purpose XADC signal/ standard Pmod · 12-bit VGA output · USB-UART Bridge · Serial Flash · Digilent USB-JTAG port for FPGA programming and communication · USB HID Host for mice, keyboards and memory sticks)	20

PRINCIPAL