Sumesh Divakaran

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Research Interests

- Program Verification
- Refinement-based Verification and Synthesis
- Model Checking
- Formal Methods

Experience

- College of Engineering Trivandrum, Kerala State, India; Professor, Computer Science & Engineering; July 2019 - till date
- Government Engineering College**,** Idukki, Kerala State, India; Professor, Computer Science & Engineering; Oct 2015 - June 2019
- Government Engineering College, Idukki, Kerala State, India; Associate Professor, Computer Science & Engineering; Aug 2009 - Oct 2015
- Rajiv Gandhi Institute of Technology, Kottayam, Kerala State, India; Assistant Professor, Computer Science & Engineering,; Jan 2006 - Aug 2009
- Rajiv Gandhi Institute of Technology, Kottayam, Kerala State, India; Lecturer, Computer Science & Engineering; Mar 2004 - Dec 2005
- University College of Engineering, Thodupuzha, Kerala State, India; Lecturer, Computer Science & Engineering; Aug 2001 - Jun 2003

Education

- Ph.D., Computer Science & Engineering, 2015, Indian Institute of Science, Bangalore, India; Advisor: Prof. Deepak D'Souza.
- ME, Computer Science & Engineering, 2009, Indian Institute of Science, Bangalore, India; Advisor: Prof. Deepak D'Souza.
- BTech., Computer Science & Engineering, University College of Engineering, Thodupuzha, India.

Collaboration

- I was an investigator for a research project funded by the Royal Academy of Engineering London. This project includes collaborators from University of York, UK, Indian Institute of Science, Bangalore, IIIT Bangalore and Mathworks India Private Limited. The period of the project was from March 2016 to March 2018.

- During my deputation for PhD at the Indian Institute of Science, Bangalore I have worked

on a joint project in the period 2010-12, sponsored by UKIERI with investigators from University of York, UK and General Motors India Ltd. As part of this project we developed a theory and framework for verifying the kernel of a real-time operating system namely FreeRTOS.

- During my deputation for PhD at the Indian Institute of Science, Bangalore I have worked on another joint project in the period 2012-15, sponsored by Robert Bosch Center for CPS, IISc with investigators from University of York, UK and Cleaveland State University, US. As part of this project we have verified the scheduler-related functionality of FreeRTOS.

Teaching

- Automata Theory and Computability

Courses Taught

- Program Analysis and Verification
- Formal Methods and Tools in Software Engineering
- Automata Theory and Computability
- Automated Verification
- Theory of Computation
- Design and Analysis of Algorithms
- Data Structures
- Compiler Construction
- Programming in C

Professional Activities (present)

- Member, Programme Committee, PhD Symposium, ISEC2019, 12th Innovations in Software Engineering Conference
- Chairman, e-Governance Cell, Department of Technical Education, Government of Kerala
- Member, e-Governance Core Committee, Higher Education Department, Government of Kerala
- Member, e-Governance Subcommittee, Higher Education Department, Government of Kerala
- Member, Expert Committee of e-Governance, APJ Abdul Kalam Technological University
- Member, Technical Committee, Kerala Public Service Commission
- Member, Board of Governors, Government Engineering College, Idukki.
- Member, Academic Council, Mahatma Gandhi University
- Member, PG Board of Studies for Computer Applications, Cochin University of Science & Technology
- Member, Business Advisory Committee, ASAP , Kerala
- Member, Board of Directors of Trivandrum Engineering Science & Technology Research Park
- Special Officer for Starting a new Government Polytechnic at Kanjikkuzhy, Idukki
- Mentor for Government Polytechnic College, Nedumkandam, Idukki
- Member, Vidyalaya Management Committee, Kendriya Vidyalaya, Idukki
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Professional Activities (past)

- Member, Editorial Committee, Plan for District Development, Idukki District, Kerala State
- Member, Selection Committee, One MP One Idea, Idukki District.

- Member, Committee formed by the Government, Sate of Kerala to evaluate projects for releasing grant from the Innovation fund sanctioned to the Idukki District.
- Member, Expert Visit Committee, APJ Abdul Kalam Technological University.
- Member, Organizing Committee, ICTAC 2012, International Conference on Theoretical Aspects of Computing.
- Member, PG Board of Studies, Mahatma Gandhi University
- Member, UG Board of Studies, Calicut University
- Member, Academic Council, Calicut University

Invited Talks

- xFig - an Interactive Drawing Tool, Essentials of Research - Workshop for Research Scholars at APJ Abdul Kalam Technological University, July 2018.
- Refinement-Based Verification of FreeRTOS in VCC, 2nd Symposium on Application of Formal Methods for Safety & Security of Critical Systems, Organized by ACM India, Amrita Vishwa Vidyapeetham, Feb 2018.
- Refinement-Based Verification of FreeRTOS in VCC, Winter School in Software Engineering, Organized by ACM India, TRDDC, Pune, 2017.
- Verifying C Programs in VCC, Continuing Education Programme, Defense Research and Development Organization (DRDO) – Center for Artificial Intelligence and Robotics (CAIR), Bangalore, 2016.
- Refinement-based Verification of FreeRTOS Scheduler in VCC, ICFEM 2015, Paris, France, 2015.
- Ensuring Correctness in Software Development, Short Training Programme for faculty, Government Engineering College, Thrissur, 2015.
- Efficient Refinement Checking in VCC, VSTTE 2014, Vienna Summer of Logic 2014, Austria, Vienna Technological University, 2014.
- Separation Logic: A Logic for Shared Mutable Data Structures, Indian Institute of Science, Bangalore, 2013.

Publications

- Refinement-Based Verification of the FreeRTOS Scheduler in VCC (with Deepak D'Souza, Anirudh Kushwah, Prahladavaradan Sampath, Nigamanth Sridhar and Jim Woodcock) in Proc. ICFEM 2015.
- Efficient Refinement Checking in VCC (with Deepak D'Souza and Nigamanth Sridhar) in Proc. VSTTE 2014.
- Conflict-Tolerant Real-Time Specifications in Metric Temporal Logic (with Deepak D'Souza and Raj Mohan Matteplackel), in Proc. TIME 2010.
- Conflict-tolerant specifications in temporal logic (with Deepak D'Souza and Raj Mohan Matteplackel), in Proc. ISEC 2010.

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