QUOTATION EXTENSION NOTICE

Quotation Number	16/P4/2020/CET/ECE
Due date and time for receipt of quotations	08/02/2021, 2 PM
Date and time for opening of quotations	10/02/2021, 2 PM
Date up to which the rates are to remain firm for acceptance	10/08/2021
Designation and address of officer to whom the quotation is to be addressed	The Principal, College of Engineering Trivandrum, Thiruvananthapuram-16. GSTIN:32AAAGC0358L1ZP
Superscription : Purchase of Equipments in the VLSI Lab of ECE Department of this institution.	

Sealed quotations are invited for the supply of the materials specified in the list attached given below/overleaf. The rates quoted should be for the delivery of the articles at the places mentioned below the schedule. The necessary superscription, due date for the receipt of quotations, the date up to which the rates will have to remain firm for acceptance and the name and address of officer to whom the quotation is to be sent are noted above. Any quotation received after the time fixed on the due date is liable to be rejected. The maximum period required for delivery of the articles should also be mentioned. Quotations not stipulating period of firmness and with price variation clause and/or 'subject to prior sale' condition are liable to be rejected.

The acceptance of the quotations will be subject to the following conditions.

1. Withdrawal from the quotation after it is accepted or failure to supply within a specified time or according to specifications will entail cancellation of the order and purchases being made at the offerers expenses from elsewhere, any loss incurred thereby being payable by the defaulting party. In such an event the Government reserves also the right to remove the defaulter's name from the list of Government suppliers permanently or for a specified number of years.

2. Samples, duly listed, should be forwarded if called for under separate cover and the unapproved samples got back as early as possible by the offerers at their own expenses and the Government will in no case be liable for any expenses on account of the value of the samples or their transport charges, etc. In case, the samples are sent by railway, the railway receipt should be sent separately, and not along with the quotation since the quotation will be opened only on the appointed day and demurrage will have to be paid if the railway parcels are not cleared in time. Quotations for the supply of materials are liable to be rejected unless samples, if called for of the materials tendered for are forwarded. The approved samples may or may not be returned at the discretion of the undersigned. Samples sent by V.P.Post or "freight to pay" will not be accepted.

3. No representation for enhancement of price once accepted will be considered during the currency of the contract.

4. Any attempt on the part of tenderers or their agents to influence the Officers concerned in their favour by personal canvassing will disqualify the tenderers.

5. If any license or permit is required, tenderers must specify in their quotation and also state the authority to whom application to be made.

6. In cases where a successful tenderer, after having made partial supplies fails to fulfill the contracts in full, all or any of the materials not supplied may, at the discretion of the Purchasing Officer be purchased by means of another tender/quotation or by negotiation or from the next higher tenderer who had offered

to supply already and the loss, if any, caused to the Government shall thereby together with such sums as may be fixed by the Government towards damages be recovered from the defaulting tenderer

7. a) Ordinarily payments will be made only after the supplies are actually verified and taken to stock but in exceptional cases, payments against satisfactory shipping documents including certificates of Insurance will be made up to 90 per cent of the value of the materials at the discretion of Government. Bank charges incurred in connection with payment against documents through bank will be to the account of the contractor. The firms will produce stamped pre-receipted invoices in all cases where payments(advance/final) for release of railway receipts/shipping documents are made through Banks. In exceptional cases where the stamped receipts of the firms are not received for the payments (in advance) the unstamped receipt of the Bank (i.e. counterfoils or pay-in-slips issued by the Bank alone may be accepted as a valid poor for the payment made. b)The tenderers shall quote also the percentage of rebate (discount) offered by them in case   the payment is made promptly within fifteen days/within one month of taking delivery of stores.

8. Any sum of money due and payable to the successful tenderer or contractor from Government shall be adjusted against any sum of money due to Government from him under any other contracts.

9. Special conditions, if any, printed on the quotation sheets of the tenderer or attached with the tender will not be applicable to the contract unless they are expressly accepted in writing by the purchases.

10. GST number must be mentioned in the quotation. The firm under composition scheme must mention the words "Composition taxable person" in their quotation and should submit proof for that.

11. The items should be supplied at **ECE Department** of this institution.

12. The unit price, all other charges such as delivery, transporting, loading and unloading charges, and GST must be shown separately in the quotation

13. Warranty: 3 years.

List of Items

1.

Sl No	Item	Quantity
1	Artix-7 FPGA : XC7A35T-ICPG236C	4
2	Zybo Z7:Zynq-7000 ARM/FPGA SoC Development Board	1

SD/-

PRINCIPAL

SL NO	NAME OF COMPONENTS	Quantity
1	**Artix-7 FPGA : XC7A35T-1CPG236C** (33,280 logic cells in 5200 slices (each slice contains four 6-input LUTs and 8 flip-flops） 1,800 Kbits of fast block RAM） Five clock management tiles, each with a phase-locked loop (PLL)） 90 DSP slices） Internal clock speeds exceeding 450MHz） On-chip analog-to-digital converter (XADC)）)	**4**
2	**Zybo Z7: Zynq-7000 ARM/FPGA SoC Development Board** (• ZYNQ Processor • 667 MHz dual-core Cortex-A9 processor • DDR3L memory controller with 8 DMA channels and 4 High Performance AXI3 Slave ports • High-bandwidth peripheral controllers: 1G Ethernet, USB 2.0, SDIO • Low-bandwidth peripheral controllers: SPI, UART, CAN, I2C • Programmable from JTAG, Quad-SPI flash, and microSD card • Programmable logic equivalent to Artix-7 FPGA • Memory • 1 GB DDR3L with 32-bit bus @ 1066 MHz)	**1**