College of Engineering Trivandrum, Thiruvananthapuram

NOTICE INVITING TENDER

P3/4639/19/CET 26.02.2020

Tender No.	**:10/2020/P3/EEE**
E-Tender ID	**:2020_DTE_342611_1**
Superscription	:Purchase of Equipments for Power System Lab of Electrical Engineering Department of this institution
Last date and time of receipt of tender on the website (www.etenders.kerala.gov.in)	:20/03/2020 3 PM
Date and time of opening of tender	:23/03/2020 11 AM
Date up to which the rates are to be firm	:30/9/2020
Tender Cost	:Rs.3304/-(Rs.2800/-+18% GST)
EMD required	:Rs.18312/-
Address of the Officer to whom hardcopy is to be send.	:THE PRINCIPAL, COLLEGE OF ENGINEERING TRIVANDRUM, THIRUVANANTHAPURAM-695016, GSTIN:32AAAGC0358L1ZP

General conditions

1.The price quoted should be inclusive of all taxes, freight charges, unloading charges, installation and commissioning charges and should be furnished unambiguously.

2.Payment: 100 % after successful supply, installation, commissioning and demonstration.

3.Delivery Period: Maximum Delivery period will be 60 days from the date of receipt of supply order.

4.Agreement as per NIT 2 in Rs.220/- Kerala Stamp Paper and tender form should be uploaded.

5.5% security deposit along with agreement should be furnished within a month/fortnight from the date of receipt of supply order.

6.Date of opening of tender: In case the proposed date declared as holiday, the tender will be opened on the next working day.

7.After E-Tendering the hard copy of all documents such as agreement, brochure, should be submitted before the opening date.

8.Warranty: 5 years for all items and should follow AMC as per existing rules.

NB: The Tender procedure will be made as per Rules mentioned in the Revised Store Purchase Manual.

The bidders should participate this tender through E-Tendering System. Tender cost and EMD should be submitted only through online. For more details Contact Ph.0471 2577088, 0471 2577188, 0471 257388, 0471 2515760.

Specifications of OP4510 Real Time simulator

General Specifications

Power supply

Universal input and active power factor correction 350W

FPGA

Kintex-7 FPGA, 325T, 326,000 logic cells, 840 DSP slice (Multiplier- adder)

Computer

8GB RAM. Xeon 4 core CPU,3.5 GHz, solid state hard disk 128 GB

Fast optical interface

4 sockets for optional Small Form-factor Pluggable (SFP&SFP+) 1 to 5 Gbits/s optical cable pairs (Rx/Tx)

Software compatibility (CPU)

Intel C++ compiler, RT-LAB multi-processors platform RT LAB 11.x host/workstation license-professional, RT LAB 11.x real time target license-B series(all RT cores activated)LINUX OS with real time kernel Simulink, RTW, SimPowerSystems, SimScape, ARTEMIS,RT-EVENT, HYPERSIM and several third-party software compatible with Simulink

FPGA XILINX System Generator for Simulink, RT-LAB XSG, eHS FPGA electrical circuit solvers, library of floating point functions, resolvers and Finite-Element based motor models and converters

Firmware: OP4510 Generic bitstream for static digital IO

e HS x32 -power electronics simulation tool box for OP 4510 simulators

generic and reprogrammable FPGA based electrical solver

Developement license

Performance

Minimum time step of 7 microseconds for model subsystems executed on the INTEL CPU and 250 nanoseconds for models executed on the FPGA chips, 10 nanosecond timer resolution

Dimensions & weight

43.2 (W) x 27.4(D) x 8.9cm (H) (17” x 10.8” x 3.5”)

5Kg (11lbs) approx, for laboratory use

AVAILABLE I/O SYSTEMS

TYPE B MODULES

Digital output card

32 channels, push-pull, 65 nanosecond typical propagation delay, 5V to 30 V adjustable by an external voltage supplied by users 200 ns to 65 ns, 32 static digital output.50 mA max, short-circuit protected, Galvanic isolation

Digital input card

32 channelsoptocouplers, 4.5V to 50V,32 static digital input. 3.5mA min, 40 nanosecond typical propagation delay, galvanic isolation with fast Opto-couplers

Analog input card

16 channels 500kS/s, 16 bits, 2.5 microsecond conversion time for all channels simultaneously, +-20V true differential input, 400 k Ohms input impedance, conversion time directly controlled by the FPGA chip

Analog output card

16 channels(1 Ms/s, 16 bits, 1.0 microsecond update time for all channels simultaneously, ± 16V, 15 mA (20 mA with option- al fast driver), short-circuit protected, update time directly controlled by the FPGA chip

Dual port-PCI EX1 Gigabit ethernet kit for OP4510 v2
RS 422 expansion board for OP4500
6RX= 6digital IN or6 PWM IN or 2 encoder IN
6 TX= 6 Digital out or 6 PWM out or 2 encoder OUT
DB9 Test loop back cable
Driver- IEC 61850 – 8-1 GOOSE Communication protocols(Publisher and Subscriber) for protection relay interface. 50 data points included
Driver IEC 65810-9-2 Sampled value communication protocol(publisher and subscriber) for protection relay interface 50 data points included

On-Board Channels

Digital input/ output RS422 (optional fiber optic) 6 channels for decoder and 6 channels for encoder or other applications requiring reading or generation of fast differential logic signals, 5V, 40 nanosecond delay typical, galvanic isolation

Sd/-
PRINCIPAL